A STUDY OF VARIOUS FORMS OF CdS SOLAR CELLS

by

P. C. PANDE

Presented in candidature for the degree of

Doctor of Philosophy

in the

University of Durham

August 1984

This thesis is dedicated to my late father

CONTENTS

ABSTRACT

The work reported in this thesis involves a study of various forms of CdS, viz. single crystal, thin and thick films deposited by electrophoresis, silk screen printing or thermal evaporation, for their potential use in fabricating photovoltaic devices by the dry barrier process, which is considered the most suitable for thin film devices. $Cd_{1-y}Zn_yS$ mixed crystals and layers have also been investigated. The electrical and structural properties of the various forms of substrate depend on their preparational parameters which in turn are reflected in the characteristics of the cells fabricated on them. With each form of material, therefore, the preparative conditions were first studied to obtain a suitable substrate for the subsequent formation of a $Cu_{2.0}S$ (chalcocite) layer, the desired phase of Cu_xS for producing efficient cells. The spectral responses of these devices, coupled with structural information deduced from Reflection High Energy Electron Diffraction patterns revealed that photo-response measurements made at 85 K give a more accurate assessment of the phase of Cu_xS. The effects occurring at the interface during heat treatment were found to be dependent on the ambient and on the nature of the substrate used for the fabrication of the device. Infra-red quenching of photocapacitance revealed the diffusion of copper into CdS where it forms acceptors with ground and excited hole states 1.1 and 0.35 eV above the valence band. Heating in air leads to additional acceptor-like states at the interface, 0.2 eV below the conduction band. Other traps were also identified in these substrates from photocapacitance studies. In devices formed on mixed crystals, a recombination centre lying ~ 1.27 eV above the valence band was found to account for the reduction in the short circuit current. A similar feature was observed in devices formed on indium doped silk screen printed CdS films. More interestingly a prominent feature was the presence of a trap 0.946 eV below the conduction band in the thermally evaporated films deposited on Ag/Cr coated glass. This trap seems to inhibit the diffusion of copper, and may help to explain the excellent maintenance properties of cells prepared on Ag/Cr coated glass.

ACKNOWLEDGEMENTS

I wish to express my thanks for the valuable guidance, constant encouragement and consistent help given by my supervisor, Dr. J. Woods. I am also grateful to Dr.G.J. Russell for constructive suggestions, many discussions, as well as for his help in the use of the transmission and scanning electron microscopes.

I would also like to thank Professor G.G.Roberts for allowing me to use the facilities of the Department of Applied Physics and Electronics, University of Durham. The help of the workshop staff,headed by Mr.F.Spence, is gratefully acknowledged.

I am particularly indebted to Mr.N.F. Thompson for his technical assistance in growing the single crystals used in this study, and for skillfully drawing the diagrams included in this thesis. I would like to express my appreciation to Mr. T.Harcourt for cutting and polishing the single crystals and to Mr. C. Pearson for general technical assistance.

I am especially grateful to Mr. A.E.Thomas for his help in preparing CdS powders for depositing electrophoretically and silk screen printed films, his advice on experimental techniques and assistance with the proof reading of this thesis. In this connection I would like to acknowledge the contribution of Dr. I.D. McInally in preparing the electrophoretically deposited samples used in this study. Also, I wish to express my thanks to Dr. A.W.Brinkman and other members of the group and the department who rendered me their help during the course of this work in one way or another.

I wish to express my gratitude to Mrs. S.Mellanby for her patience whilst typing this thesis. I also extend my acknowledgements to the Association of Commonwealth Universities, London, and the Ministry of Education and Culture, Govt. of India, for the award of the Commonwealth Scholarship to enable me to carry out this work.

CHAPTER 1

INTRODUCTION

1.1 IMPORTANCE OF PHOTOVOLTAIC CELLS FOR TERRESTRIAL USE

The fast depletion of the world's non-renewable fossil fuel resources has created a need for finding an alternative. With the onset of the energy crisis in 1973 greater interest was taken towards developing independent and inexhaustible sources of energy. Solar energy is considered to be one of the most promising alternative sources. It is abundant and non polluting. In nature solar energy is utilised by plants through photosynthesis, and is stored in the form of biomass. Wind and ocean energies are also manifestations of the sun's energy. Technologically solar energy can be harnessed either in the form of thermal energy by using flat plate collectors and concentrators, or by generating electricity using photovoltaic cells. The latter approach finds more use, particularly in developing countries where the possibility of the electric grid extending to remote areas is bleak in the near future. As an example, in countries with agricultural based economies and high solar insolation, the potential importance of solar powered pumps for use in irrigation is obvious. Encouraging results have been obtained in exploratory trials to investigate the practical feasibility of this application of photovoltaics[1]. Besides this, solar cells are useful in running television sets for educational programmes, and refrigerators for keeping medicines in isolated village health centres. In general, depending upon the cost of production of photovoltaic cells, their application can be extended to public utilities, in order to supplement the peak power demand.

1.2 BRIEF HISTORY

The concept of the photovoltaic cell is an old one. As long ago as 1839 Becquerel [2] discovered that a photovoltage resulted from the action of light on an electrode in an electrolyte solution. This was followed by similar observations in 1877 by Adams and Day[3] in the solid material selenium, shortly after Smith[4] had demonstrated the phenomenon of photoconductivity in selenium. Subsequently some pioneering work was performed on selenium and cuprous oxide photovoltaic cells by Lange[5], Grondahl[6] and Schottky[7]. This work eventually resulted in the photo-electric exposure meter which was used up to the 1950's. The photo-voltaic effect was successfully differentiated from the Dember effect[8], which is the production of a potential difference across a photoconductor by non-uniform illumination.

The modern history of solar cells originates in 1954 when Chapin et al[9] reported a 6% efficient silicon single crystal solar cell. In the same year Reynolds et al[10] obtained a reported 6% efficiency in CdS solar cells. Jenny et al[11] produced a 4% GaAs solar cell in 1956. At that time the importance of photovoltaic cells was mainly in the space programmes, and the prime focus of research was to increase the efficiency and reliability of the cells. Particular attention was paid to solving the problem of radiation damage to the cells in the space. CdS solar cells were considered to be more radiation resistant[12] and their use in thin film form offered the prospect of enhancing the power to weight ratio. However, these CdS cells failed to reach a sufficiently high efficiency to compete with single crystal silicon cells (efficiency $\sim$ 15-17%)[13,14] and GaAs based devices (efficiency approaching 22%)[15,16] for which production costs remained very high. In view of the recent interest in utilising photovoltaic cells for terrestrial purposes, reducing their cost has become the primary aim. To achieve this, improvements in the technology and an increased scale of production of single crystal silicon solar cells

were given priority. Annual commercial production was increased 500 percent over three years, from a total generating capacity of 3 megawatts of electricity in 1980 to a capacity rated at nearly 18 MW in 1983. This led to modules of about 12% efficiency costing \$7/Wp[17]. At the same time much attention was given to the more promising thin film solar cells. These require less material and energy for their fabrication than single crystal cells. Several materials were investigated for use in thin film solar cells, e.g. amorphous silicon, II-VI compounds (CdS, CdTe, CdSe), III-V compounds (InP, GaAs), ternary compounds ($Cd_{1-y}Zn_yS$) and II-III-VI_2 compounds ($CdInSe_2$)[18]. Recently, Zn_3P_2 has also been considered as a promising material [19].

Amorphous silicon solar cells have been produced commercially and used for low grade electronic devices[20]. CdS/Cu_2S solar cells which had been beset by degradation problems initially, have now been stabilized and large production is being undertaken by Nukem[21]. The basic principles, the chronological details of the development and the state of art of photovoltaic cells have been reviewed from time to time in a number of articles[12,23-28], special issues of Journals[29-31] and books[32-39]. Some of the important features are summarised in the following section.

1.3 THE SOLAR CELL

1.3.1 Choice of Material

The essential features of a solar cell are an absorber generator material in which mobile carriers are created by the absorbed solar energy and a built-in voltage which allows the generated carriers to be collected from the region in which they are produced and converted to majority carriers. The purpose of the collector converter is to prevent the back flow of carriers. The absorber region controls the magnitude of the current that is generated and the height of the potential barrier determines the voltage that the cell can produce. Obviously to produce more photocurrent, the bandgap of the

semiconductor should be small, while on the other hand, in order to obtain high open circuit voltage a large value of bandgap is preferable. When these two factors are matched with the solar spectrum, the optimum value of bandgap of the material has been determined to be between 1.2-1.5 eV[40,41]. Fig (1.1) represents the maximum conversion efficiency obtainable for solar cell absorber generator material as a function of energy gap. It is obvious that CdTe with bandgap 1.44 eV, GaAs (1.34 eV), InP(1.27 eV) and Cu_2S(1.2 eV) are most promising materials.

The generator material should have a high value of absorption coefficient to ensure capture of all available photons. The absorption coefficient of a few materials are shown in Fig 1.2. When the spectral density is convoluted with the absorption coefficient of the materials suitable for photovoltaic cells, one finds that Cu_2S will absorb 90 percent of the sunlight above its energy gap with a thickness of only 0.4 μm, while silicon needs 100 μm thickness to absorb 90 percent of the photons[42].

The generated carriers must be mobile and must continue in their separated state for a time that is long compared with the time they require to travel to the localized charge separating inhomogeneity. This process is characterised in terms of the carrier diffusion length, which maybe viewed as the distance over which the photogenerated carrier density decreases by e^{-1} as the carriers move by diffusion. The diffusion length increases as the square root of the product of the recombination lifetime and mobility of the carriers. The recombination lifetime depends on the capture cross section and density of defects. The mobility of the carriers, in turn, depends on the scattering mechanisms present. All of these parameters depend on temperature, the impurity concentration, crystallinity, crystal orientation and type of defect. It is estimated that to transport 90 percent of the generated minority carriers to the junction, the diffusion length should be twice the absorber film thickness[24]. For most of the materials shown in

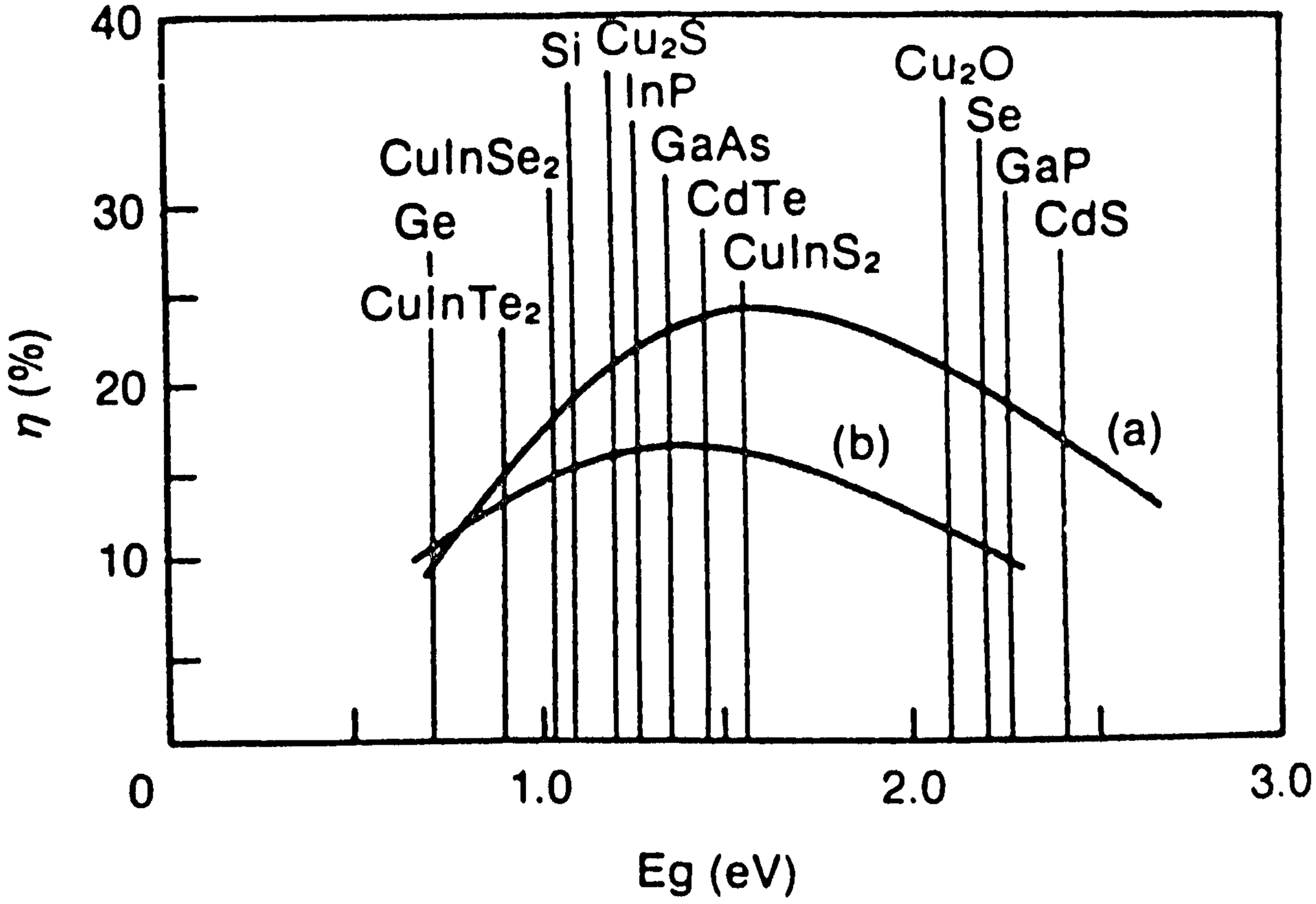


FIGURE 1.1: Dependence of efficiency on semiconductor band gap
(a) for A = 1 for injection dominated current regime and
(b) for A = 2 for the regime dominated by the recombination in the depletion layer (Ref 41)

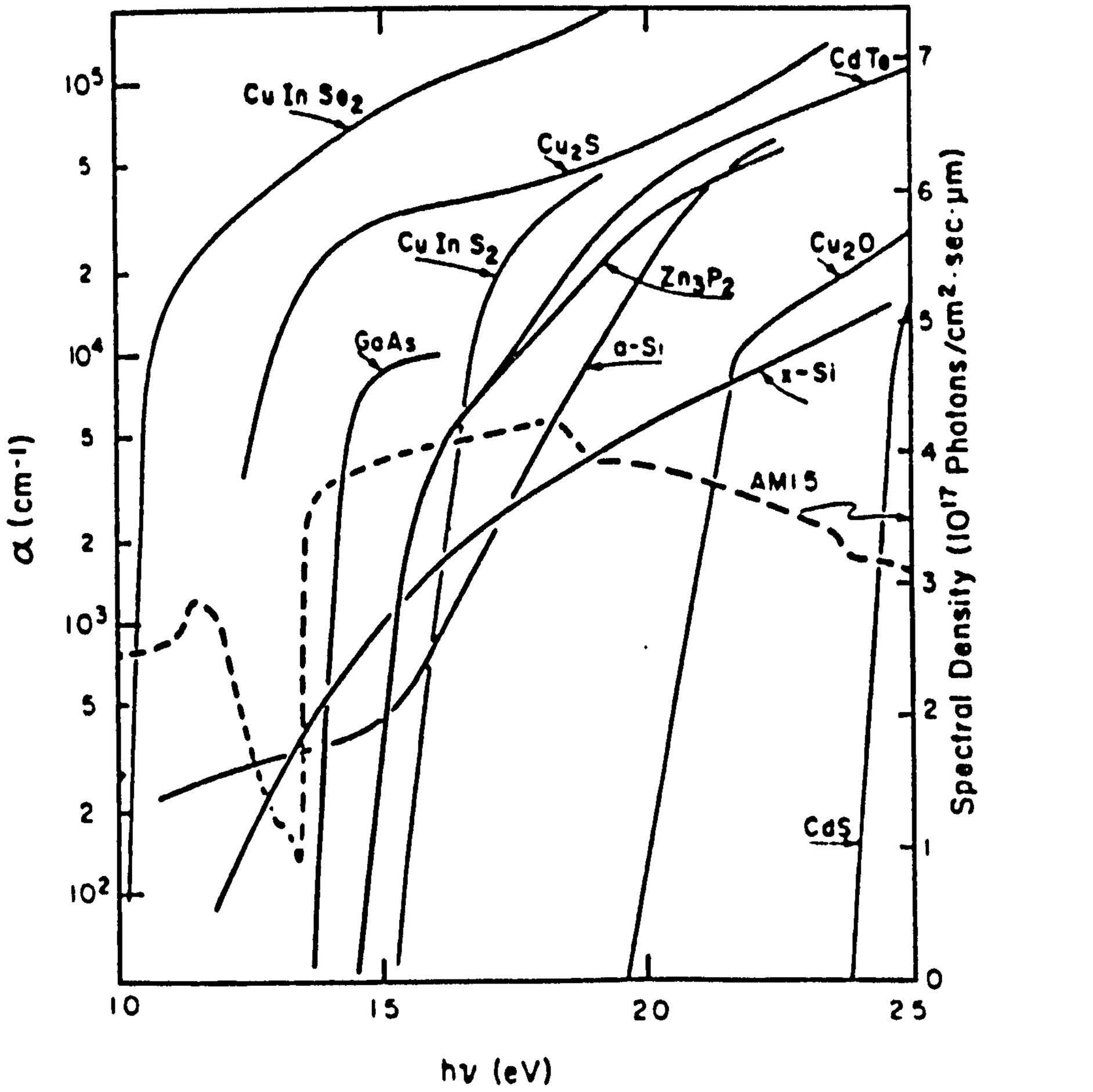


FIGURE 1.2: Optical absorption coefficient versus photon energy for typical solar cell materials (Ref 42)

Fig (1.2) with an energy gap between 1.0 and 1.7 eV, the diffusion lengths have been observed to be twice the effective absorption length except for amorphous silicon where the photon absorption and minority carrier generation occurs in the space charge region and the built in electric field is used to transport the minority carriers.

1.3.2 The Junction

The internal electric field within the semiconductor is created by an electronic inhomogeneity which can be achieved either by providing a metal semiconductor contact (Schottky barrier) or by forming a p-n junction between two regions of a semiconductor (homojunction) or a junction between two different semiconductors (heterojunction). Schematic diagrams of these different types of junction and their corresponding band diagrams are shown in Fig 1.3.

Homojunctions have the advantage that their theory has been studied in great detail because of their applications in rectifiers and transistors. Some metallurgical and electronic problems such as the matching of thermal expansion coefficients,lattice constants and electron affinities do not arise in these junctions. However, appreciable losses of the mobile carrier take place due to front surface recombination. Since only a few materials can be doped both p and n-type, useful homojunctions are limited to single crystal silicon, amorphous and polycrystalline silicon, gallium arsenide and cadmium telluride.

A heterojunction solar cell consists of a small band gap semiconductor (absorber generator) in which optical absorption takes place and a large band-gap material (collector converter) that acts as a window for the junction. If the two semiconductors have the same type of conductivity the hetero-junction is called isotype, otherwise it is known as anisotype. Such hetero-junctions can also be classified as abrupt or graded according to the distance in which the transition from one material to the other is completed near the

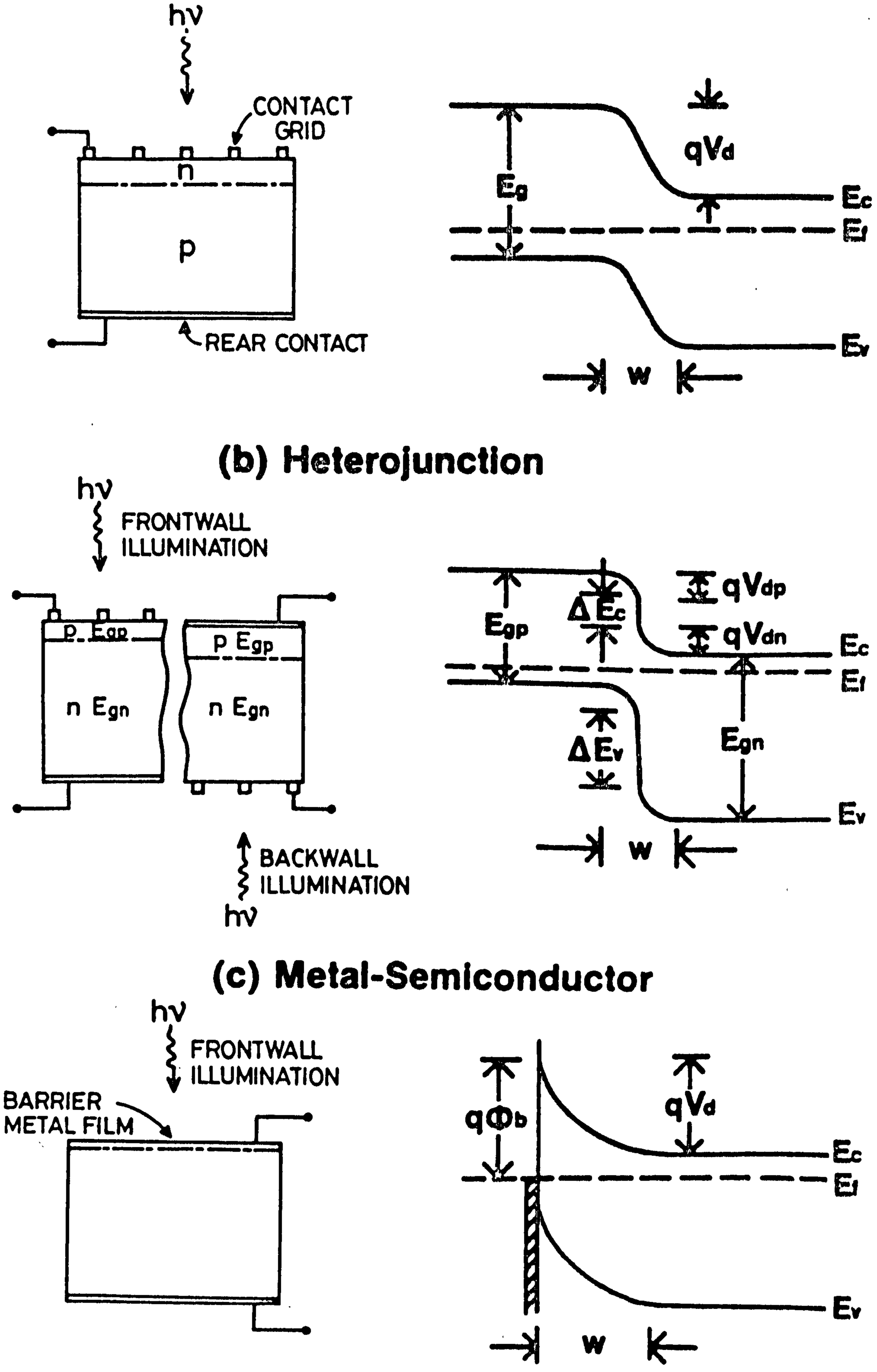


FIGURE 1.3: Diagramatic illustrations of different types of solar cells

interface. The primary advantage of a heterojunction structure is that it allows various materials to be used which cannot be doped both p and n-type but have other outstanding features. Moreover the junction can be operated in front-wall or back-wall modes (see Fig 1.3). A suitable material is chosen for the absorber generator which has all the characteristics discussed in the preceding section. For the collector converter the band-gap should be as large as possible while maintaining a low series resistance. The other important factors are the lattice constants and electron affinities of the two semiconductors. A high density of interface states is introduced by the lattice mismatch between the two semiconductors, and band discontinuities develop because of the difference in electron affinities. With the proper choice of a ternary compound (e.g. $Cd_{1-y}Zn_yS$ instead of CdS in a CdS/Cu_2S junction) as collector converter, these drawbacks can be overcome and a heterojunction can exhibit the optimum properties of a homojunction without the problem of front surface recombination loss. Quarternary compounds such as $Al_xGa_{1-x}As_yP_{1-y}$ and $Cu_xIn_{1-x}Se_yTe_{1-y}$ yield two degrees of freedom and ideally both the bandgap and lattice constant can be adjusted to give an optimum junction.

The positive aspects of homojunctions and heterojunctions are combined in heteroface structures in which the free surface of a homojunction is replaced with a large bandgap window material so that the original free surface recombination velocity is replaced by an interface recombination velocity which is several orders of magnitude smaller. The most common heteroface structure is the $Al_xGa_{1-x}As/GaAs$ solar cell.

The Schottky barrier has the advantage of ease of preparation since it does not require diffusion processes to be carried out at elevated temperature, and a simple blocking contact is formed. Performance of these devices is usually limited by large thermionic emission currents that reduce

the open circuit voltage. Recently Metal Insulator Semiconductor (MIS) and Semiconductor (SIS) junctions have received much attention. These are equivalent to Schottky barrier and heterojunction systems respectively, with the addition of a thin layer of insulator usually an oxide at the interface to reduce the forward current. 7% efficient MIS devices have recently been made on CdSe and these are considered promising[43].

The selection of material and type of junction also requires an investigation of the availability of materials, cost, material toxicity, cell stability and lifetime. It should also be possible to form low resistance electrical contacts to both n and p type materials. Since all the semiconductor materials used for solar cells have high refractive indexes ($\sim$ 2-4), 25-35% of the incident radiation is reflected from the planar surface. Antireflection coatings are used to minimize these losses. Generally the surface is textured and then a layer of AR coating is applied. SiO_2 has successfully been used on Si and CdS/Cu_2S solar cells. A layer of TiO_2 is used in GaAs devices[18]. Finally, the cell should be well encapsulated to protect the solar cell from the environment.

From these considerations it is clear that only a few limited materials can be used for solar cells. Some of these are listed in Table 1.1 together with the efficiency of the resultant solar cells. Besides silicon or gallium arsenide cells other devices which have shown promise are InP/CdS (15%)[44], InP/ITO (14.4%)[45], $CuInSe_2$/CdS(12%)[46], CdTe/CdS(12%)[47], Cu_xS/CdS(9.1%)[48], $Cu_xS/Cd_{1-y}Zn_yS$(10.2%)[49] and amorphous silicon (10%)[50]. Of these the last five have been fabricated in the form of thin films. However, their efficiencies are still limited and have values which are much below the theoretical maximum.

A recent concept to increase the efficiency is that of Cascade/Tandem solar cells. Since a single semiconductor utilizes only a limited portion of the incident solar spectrum and the open circuit voltage of the device is

TABLE 1.1: Illustrative Photovoltaic Systems and Parameters (From Ref 38).

Description of Cell	V_{oc}	Solar Efficiency %(AM1)
Single crystal Si homojunction	0.63	16.8
Polycrystalline Si	0.57	9.5
Al/Si MIS junction	0.45	8
Au/Si MIS junction	0.55	9
Indium tin oxide/Si junction	0.51	12
Pt.Schottky barrier on amorphous Si	0.80	5.5
Single crystal GaAs p/n homojunction	0.97	20
Single crystal AlGaAs/GaAs junction	0.9	22
Au/GaAs MIS junction	0.73-0.83	15-17
Au/GaAs MIS junction on polycrystalline GaAs	0.62	3.5
CdS/Cu_2S junction on evaporated CdS	0.52	9.1
$Cd_{1-x}Zn_xS/Cu_2S$ junction on evaporated $Cd_{1-x}Zn_xS$ layer	0.6	10.2
CVD CdS on InP to form CdS/InP junction	0.79	15
Evaporated CdS on CVD InP to form CdS/InP junction	0.72	11.9
Ion beam deposited indium tin oxide on InP to form ITO/InP junction	0.76	14.4
rf sputtered ITO on CVD InP to form ITO/InP junction	0.69	12.4
CdS/CdTe junction on evaporated CdS	0.63	8
CVD CdS on CdTe to form CdS/CdTe junction	0.67	12
Spray pyrolysis CdS on CdTe to form CdS/CdTe junction	0.53-0.72	5.5-6.5
Totally screen printed CdS/CdTe junction	0.69	8.1
Evaporated CdS on $CuInSe_2$ to form $CdS/CuInSe_2$ junction	0.49	12

limited by the bandgap of the semiconductor, these two effects lead to high internal losses in conventional cells. If two or more solar cells having different semiconductor materials with suitably separated bandgap values are made one behind the other, such that the largest gap material faces the incident radiation first, the high energy photons are absorbed by the first material, and the rest of the solar spectrum falls on the second solar cell which absorbs the higher energy portion of the transmitted radiations while the remainder passes to the third one. This selective absorption process continues down to the cell with the lowest energy gap. Alternatively the incident photons are split into spectral parts by an optical filter, and each part is directed towards a separate cell which is designed to match with a specific part of the spectrum. Details of these novel concepts are summarised in Refs (38,39). Recently thin film tandem structures of CdS/Cu_2S solar cells have been described and are thought to be very promising[51]. Such a cell is expected to be 15% efficient without a substantial increase in production costs. A tentative structure for such a tandem solar cell with ZnSeTe - ZnCdS as wide bandgap parts is shown in Fig 1.4.

1.4 CURRENT STATUS OF PV SYSTEMS

The largest photovoltaic generator plant (1 MW DC) has been installed by Arco Solar Inc. in Hesperia in Southern California[17]. Several pilot plants ranging in size from 30 kW to 300 kW have been installed as demonstration projects by the Commission of European Communities. These plants are based on single crystal silicon solar cells. The location and details are summarised in Table 1.2 [52]. The experience gained with these systems can be extended to low cost solar cells which are expected to emerge from the advances in thin film technology. Hay et al[53] calculated the energy consumption in fabricating four different types of cells viz. single crystal silicon, ribbon silicon, amorphous silicon and CdS/Cu_2S. They found that

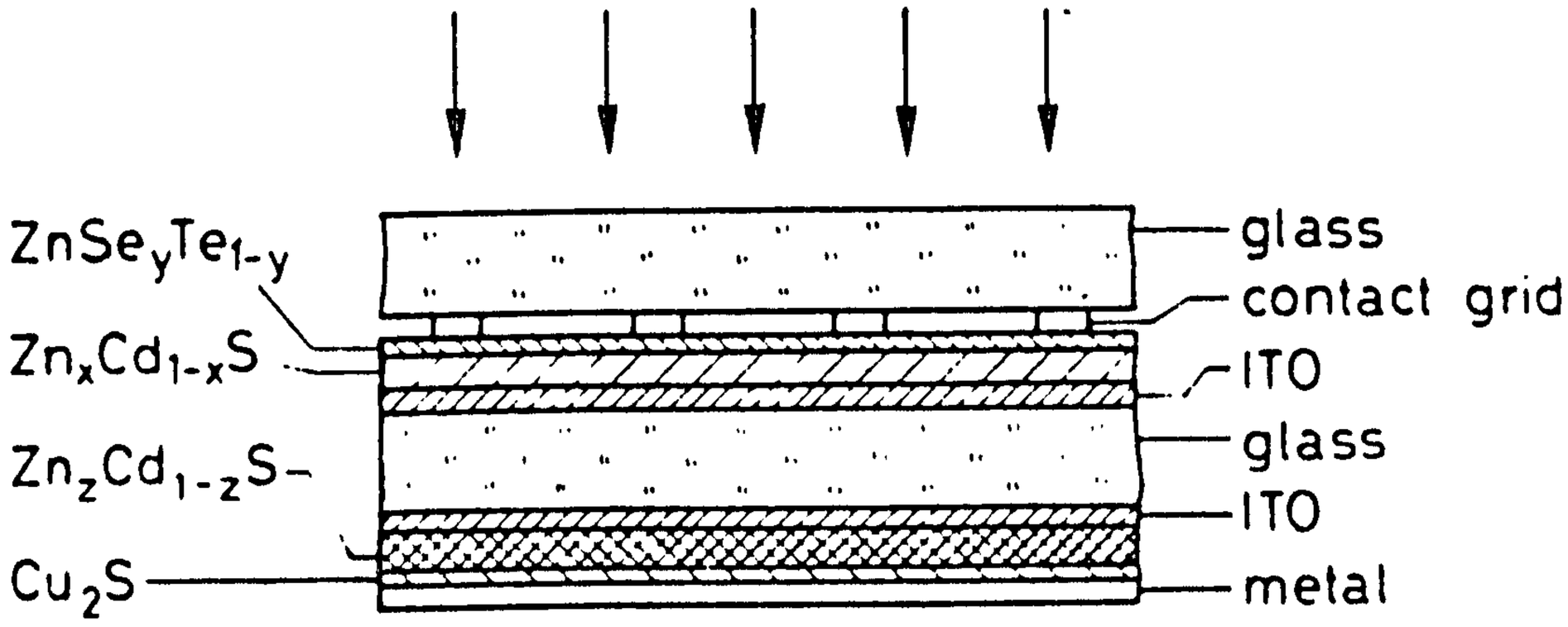


FIGURE 1.4: A schematic diagram of the structure of a $Zn_xCd_{1-x}S$-$ZnSe_yTe_{1-y}$ tandem solar cell (Ref 51).

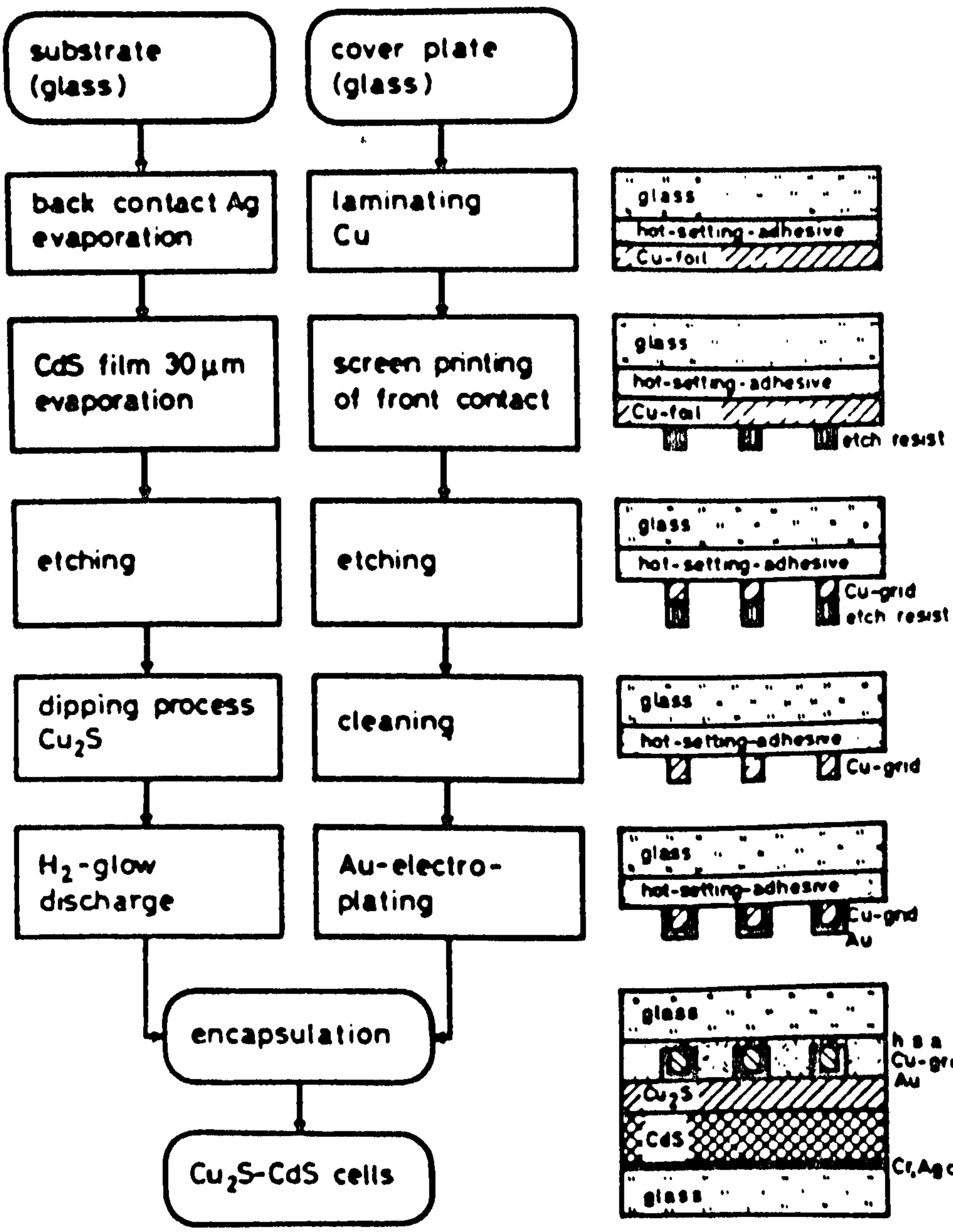


FIGURE 1.5: Schematic diagram of the process used by Nukem for the fabrication of CdS/Cu_2S photovoltaic cells (Ref 51).

TABLE 1.2: CEC Photovoltaic Pilot Projects (Ref 52).

Site		Application	Peak power kWp	Storage cap. kWh	Back-up
BELGIUM:	Chevetogne	Aux. power for swimming pool	63	380	Grid
	Hoboken	Hydrogen production	30	1600 l comp. H_2	Grid
FRANCE:	Mont Bouquet	FM & TV repeater station	50	176	Grid
	Nice	Airport power management	50	176	Grid
	Rondulinu,Corsica	Village electrification	44	360	Diesel
	Kaw,Fr.Guyana	Village electrification	35	410	Diesel
GERMANY:	Pellworm Is.	Recreational Centre	300	2076	Grid
GREECE:	Aghia Roumeli,Crete	Village electrification	50	410	Diesel
	Kythnos Is.	Village electrification	100	600	Diesel
IRELAND:	Fota Is,Cork	Dairy farm	50	160	Grid
ITALY:	Tremiti Is.	Seawater desalination	65	500	None
	Giglio Is.	Water disinfection and agricultural cold store	43	260	Grid
	Vulcano Is.	Village electrification	80	550	Diesel
NETHERLANDS:	Terschelling Is.	Marine training school	50	180	Wind gen & grid
U.KINGDOM:	Marchwood, Southampton	Power supply to grid	30	88	None

CdS/Cu_2S consumes less energy during its preparation. The most advanced stage of production in CdS/Cu_2S solar cells has been achieved by Nukem, G.m.b.H Hanau. The process of fabrication is shown in Fig(1.5). The total cost of production has been estimated to \$118 m^{-2} for a production capacity of 15,000 m^2 $year^{-1}$. With a generator efficiency of 5% the total production costs come out to be \$ 2.4 Wp^{-1}. The scaling up of the production plants to the multimegawatts range is expected to bring the production costs down to less than \$ 1 Wp^{-1}. The lowest production costs have been projected for electrophoretically deposited CdS with entirely solar processing for $CdS-Cu_2S$ modules in a low wage economy. This gives an anticipated production cost of about \$ 30 m^{-2} (54,55).

1.5 THE PRESENT WORK

The work reported in this thesis is primarily concerned with various forms of cadmium sulphide for use in the fabrication of CdS/Cu_2S solar cells by the dry barrier process in which a solid state reaction between CdS and CuCl promotes the formation of the Cu_2S layer. The study includes hetero-junctions formed on single crystals of CdS and $Cd_{1-y}Zn_yS$ and thin and thick films of CdS deposited by electrophoresis, silk screen printing and thermal evaporation. The single crystal substrates were used to optimize the preparative conditions for an efficient device. The variation of the preparative parameters, the effects of the ambient on the post-barrier heat treatment and the optoelectronic properties of the junction are described in Chapter 5. Effects occuring at the interface between CdS and Cu_2S during the heat treatment have been investigated in detail using the technique of infrared quenching of photocapacitance. Interface effects in devices formed on single crystal $Cd_{1-y}Zn_yS$ have also been studied and are described in Chapter 6. The studies of thin (1-2 μm) and thicker films (∿10 μm) of CdS deposited by electrophoresis are described in Chapter 7. It includes the assessment of the structural and electrical properties in addition to the

characteristics of the devices formed on these films. Concurrently work on silk screen printed films was also carried out. The details of the preparation of CdS and $Cd_{1-y}Zn_yS$ phosphors, as well as that of the films produced from them are reported in Chapter 8 which also includes an account of their electrical and structural properties and the effects of doping on the characteristics of devices formed on these films. Finally the effect of different preparative parameters on the structural and electrical properties of thermally evaporated CdS films and the junction properties are described in Chapter 9. Photocapacitance studies were carried out on all of the devices formed on these thin and thick film substrates in order to identify different defect centres and to evaluate their effect on the device parameters.

REFERENCES TO CHAPTER 1

1. M.R. Starr, P.L. Fraenkel and W.B.Gillet, Rural Power Sources, Conf. C 32, Newcastle Polytechnic, ISES U.K.Section, March (1983), Ed.R.Hill, p.81.

2. E. Becquerel C.R.Hebd ,Seances Acad.Sci. 9 (1839) 561.

3. W.G.Adams and R.E.Day: Proc.R.Soc.London Ser.A 25 (1877) p.113.

4. W.Smith: Nature (London) 7 (1873) p.303.

5. B.Lange, Zeit.Phys. 31 (1930), p.139.

6. L.O.Grondahl, Rev.Mod.Phys. 5 (1933) p.141.

7. W.Schottky, Zeit.Phys. 31 (1930), p.931.

8. H.Dember, Phys. Z. 32 (1931). p.554.

9. D.M. Chapin, C.S.Fuller, and G.L.Pearson, J.Appl.Phys. 25 (1954) p.676.

10. D.C.Reynolds, G.Leies, L.L.Antes and R.E.Marburger, Phys. Rev. 96 (1954) p.533.

11. D.A.Jenny, J.J. Loferski and P.Rappaport, Phys.Rev. 101 (1956) p.1208.

12. R. Hill, 'Thin Film Solar Cells' in 'Active and Passive Thin Film Devices' ed. T.J.Coutts (Academic Press 1978) p.487.

13. H.W. Brandhorst Jr: Jap.J.Appl.Phys. 16 (1977) p.399.

14. M. Wolf, IEEE Trans.Electron Devices, ED-27 (1980) p.751.

15. J. Ewan, R.C.Knechtli, R.Loo and G.S.Kamath, Proc.13th IEEE P.V.S.C. (1978) p.941.

16. R. Sahai, D.D.Edwall and J.S.Harris : Appl.Phys.Lett. 34 (1979) p.147.

17. M.A.Fischetti, IEEE Spectrum. March 1984, p.40.

18. A.Rothwarf, J.Vac.Sci.Technol. 20 (1982) p.282.

19. M. Bhusan, Proc. 4th ECPV.Solar Energy Conf(ID.Reidel:London 1982) p.844.

20. Y.Hamakawa, Proc.5th E.C.Photovoltaic Solar Energy Conf. Greece, (D.Reidel Publishing Co.Dordrecht, 1983) p.690.

21. G.H.Hewig, W.Hoffman, H.Huschka, B.Schurich and J.Worner,Proc.5th E.C.P.S.E.C Greece, (D.Reidel Pub.Co. Dordrecht, 1983) p.460.

22. P.Rappaport, RCA Rev. 20 (1959), p.373.

23. M.Wolf, Proc. 25th Ann. Power Sources Symp. Atlantic City, P.S C Public .Comm.Red.Bank.New Jersey, (1972).

24. A.Rothwarf and K.W.Boer, Prog.Solid State Chemistry 10 (1975) p.71.

25. A.G.Stanley in Applied Solid State Science Vol.5 Ed. by R. Wolfe. "Cadmium Sulphide Solar Cells" (Academic Press, London 1978)p.487.

26. K.W.Boer, J.Appl.Phys. 50 (1979). p.5356.

27. L.Kazmerski, 'Introduction to Photovoltaicsin Solar Materials Science. Ed. L.E.Murr (Academic Press, 1980).

28. R.H.Bube, 'Heterojunction for Thin Film Solar Cells' in Solar Materials Science, Ed. L.E.Murr (Academic Press, 1980).

29. H.W.Brandhorst and M.P.Godlewski eds.IEEE Trans.Electron Devices ED-24 No. (4) (1977).

30. F.A.Lindholm and P.Rappaport eds. IEEE Trans. Electron Devices ED-27 No.4 (1980).

31. T.J.Coutts, L.L.Kazmerski and S. Wagner, Eds: Solar Cells 12 (1984).

32. H.J.Hovel, Semiconductors and Semimetals Vol.11 Solar Cells. (Academic Press, New York 1975).

33. C.E. Backus, ed. 'Solar Cells' IEEE Selected Reprint Series Wiley (Inter Science) New York, 1976.

34. W.Palz: Solar Electricity,'An economic approach to solar energy', Butterworth, London 1978.

35. D.L.Pulfrey, Photovoltaic Power Generation (Van Nostrand-Reinhold, New York, 1978).

36. L.L.Kazmerski, ed. Polycrystalline and amorphous thin films and devices (Academic Press, New York, 1980).

37. S.J.Fonash, Solar Cell Device Physics,(Academic Press,New York,1981).

38. K.L.Chopra and S.R.Das, Thin Film Solar Cells (Plenum Press, New York, 1983).

39. A.L.Fahrenbruch and R.H.Bube, Fundamentals of Solar Cells, Photovoltaic Solar Energy Conversion (Academic Press, New York 1983).

40. M.B.Prince, J.Appl.Phys. 27 (1955), p.534.

41. J.J. Loferski, J.Appl.Phys. 27 (1956). p.7.

42. A.M.Barnett and A.Rothwarf, Ref.30, p.625.

43. E.Rickus, Proc.5th E.C.P.V.S.C. Greece, (1983) p.746.

44. J.L.Shay, S.Wagner, M.Bettini, K.J.Bachman and E.Buehler, IEEE Trans.Devices ED-24 (1973). p.483 .

45. K.S.Sreeharsha, K.J.Bachmann, P.H.Schmidt, E.G.Spencer and F.A.Thiel, Appl.Phys. Lett. 30 (1977), 645.

46. S.Wagner, J.L.Shay, P.Migliorato, and H.M.Kasper, Appl.Phys.Lett. 25 (1974)p434.

47. K.Yamaguchi, N.Nakayama, H.Matsumoto and S.Ikegami, Jpn. J.Appl.Phys. 15 (1976) p.1575.

48. A.M.Barnett, J.A.Bragagnalo, R.B.Hall, J.E.Phillips and J.D.Meakin, Proc.13th IEEE Photovoltaic Specialists Conf.(1978)p.419.

49. R.B.Hall, R.Birkmire, J.E.Phillips and J.D.Meakin, Appl.Phys. Lett. 38 (1981) p.925.

50. A.Catalano, R.D'Aiello, J.Dresner, B.Faughnan,A.Firester, J.Kane, Z.E.Smith, H.Schade , G.Swartz and A.Triano, Proc.16th IEEE Photovoltaic Specialists Conf., San Diego (1982), 16.A6.

51. F.Pfisterer and W.H.Bloss, Solar Cells 12 (1984) p.155.

52. F.C.Treble, Proc.5th E.C.PVSC,Greece, (1983) p.584.

53. K.Hay,J.Harrison,R.Hill and T.Riaz,Proc.15th Photovoltaic Specialist Conf.IEEE New York (1981). p.267.

54. T.J.Cumberbatch,N.M.Pearsall and R.Hill,Proc.5th PVSC, Greece(1983)p.931.

55. R.Hill, Solar Cells 12 (1984)p105.

CHAPTER 2

THE CdS SOLAR CELL

2.1 INTRODUCTION

The CdS solar cell is essentially a heterojunction which is fabricated by depositing a Cu_xS layer on to a CdS substrate and providing electrical contacts to both semiconductors. It is known as the CdS solar cell for historical reasons which go back 40 years to the time when Reynolds et al[1] reported a photovoltaic effect with an OCV of 0.45 V and SCC 15 mA/cm^2 under solar illumination from a device formed on CdS by providing a copper contact. They attributed the effect to a two step photo-excitation process through impurity levels in CdS. Since then a great deal of effort has been put into improving the efficiency of the cell and improving our understanding of the physical processes involved. Copper electrodes on CdS were also investigated by Woods and Champion[2], Williams and Bube[3], Fabricius[4] and Grimmeiss and Memming[5]. Cuong and Blair[6] found that the spectral response of a cell in the infra-red region was enhanced by two orders of magnitude under simultaneous illumination with green light. They suggested that this was due to the creation of extra minority carriers by excitation of electrons from the valence band to impurity states in the CdS. However, the work of Cusano[7], Hill and Kermidas[8], Selle et al[9] and Potter and Schalla[10] revealed that the photoabsorption takes place in Cu_xS layer. It is now established that the CdS solar cell is an anisotype heterojunction between n-CdS and p-Cu_2S[11].

The first all thin film cells were made by Nadjakov et al[12] using Al and Au electrodes. Photovoltaic effects using Cu on CdS films were also reported[13,14]. Laboratories such as Harshaw Ltd., the Clevite Corporation and RCA in U.S.A, IRD in the U.K, SAT in France, were involved

in the development of thin film cells. The major contributions came from Shirland[15] and Shiozawa et al[16]. Cells were mostly fabricated on thermally evaporated CdS layers about 30 μm thick, deposited on kapton coated with screen printed silver. The Cu_2S layer was formed by a wet chemical replacement reaction (Clevite process). The top transparent contact was a gold plated copper grid.

Extensive development of the CdS/Cu_xS cell has been carried out more recently at the Institute for Energy Conversion, University of Delaware, U.S.A.[17-19] and at the University of Stuttgart, Germany, with thermally evaporated layers of CdS[20-23]. Zinc coated copper substrates were used by the Delaware group. They claimed that zinc provides isolation of the CdS from the Cu substrate, makes an ohmic contact and after alloying with the Cu substrate provides a surface with good optical reflection. After forming the junction an additional heat treatment in vacuum or reducing atmosphere was administered to optimise the efficiency. The Stuttgart group used Ag/Cr coated glass as the substrate and found that silver reduced the degradation in the cells. Other processes such as passing a H_2 glow discharge or a short heat treatment in air were also recommended to check the degradation effects which had earlier thwarted the successful application of CdS solar cells.

Several other fabricational processes have been used to form CdS/Cu_2S cells. These include formation of CdS films by spray pyrolysis, sputtering, silk screen printing or electrophoresis, and forming junctions by a variety of techniques including the wet chemical replacement reaction, a solid state exchange reaction (dry barrier process), chemical deposition and thermal evaporation of Cu_xS. These different processes together with the properties of CdS and Cu_xS and the models which have been proposed to explain the CdS/Cu_2S solar cell, have been reviewed by Shirland[15], Stanley (1975)[24], Hill (1978)[25], Savelli and Bougnott (1979)[26], Rothwarf (1980)[27],

Martinuzzi (1981)[28], Boer[29,30], and recently by Fahrenbruch and Bube[31]. Some of the more important features are described in this chapter.

2.2 PROPERTIES OF CADMIUM SULPHIDE

Cadmium sulphide is a IIb-VIb semi-insulating compound which crystallizes normally in the hexagonal wurtzite form and has a direct bandgap of about 2.4 eV giving it a transparent yellow appearance. Under certain growth conditions, a metastable cubic sphalerite structure may predominate[32-34]. The wurtzite and cubic structure are both characterised by tetrahedral sites and as a consequence their nearest neighbour environment is identical, but positional and directional differences exist beyond the next nearest neighbours (Figs 2.1a,b). The wurtzite structure consists of two interpenetrating hexagonal lattices displaced with respect to each other by a distance of 3c/8 along c axis (Fig 2.1a). The cubic sphalerite structure is composed of two face centred cubic lattices translated with respect to each other by one quarter of the body diagonal (Fig 2.1b).

CdS starts to sublime at 700°C and melts at above 1500°C under several atmospheres pressure. It is possible to grow cadmium sulphide from the melt using a high pressure autoclave[35], but it is easier to grow crystals from the vapour phase. This lattertechnique has been employed extensively in the laboratory.

The resistivity of pure crystals of cadmium sulphide is very high. In the dark and at room temperature the mobility of electrons is approximately 300 $cm^2\ V^{-1}\ sec^{-1}$ in good crystals, whereas the hole mobility is about 20 $cm^2\ V^{-1}\ sec^{-1}$. In single crystals, the mobility is limited by ionized impurity scattering at low temperatures and polar optical mode scattering at higher temperatures. In thin films there may be additional geometrical effects limiting mobilities, and intergranular boundaries are also important.

Cadmium sulphide has been extensively studied over the last three decades and has been found to exhibit many interesting phenomena, e.g. high

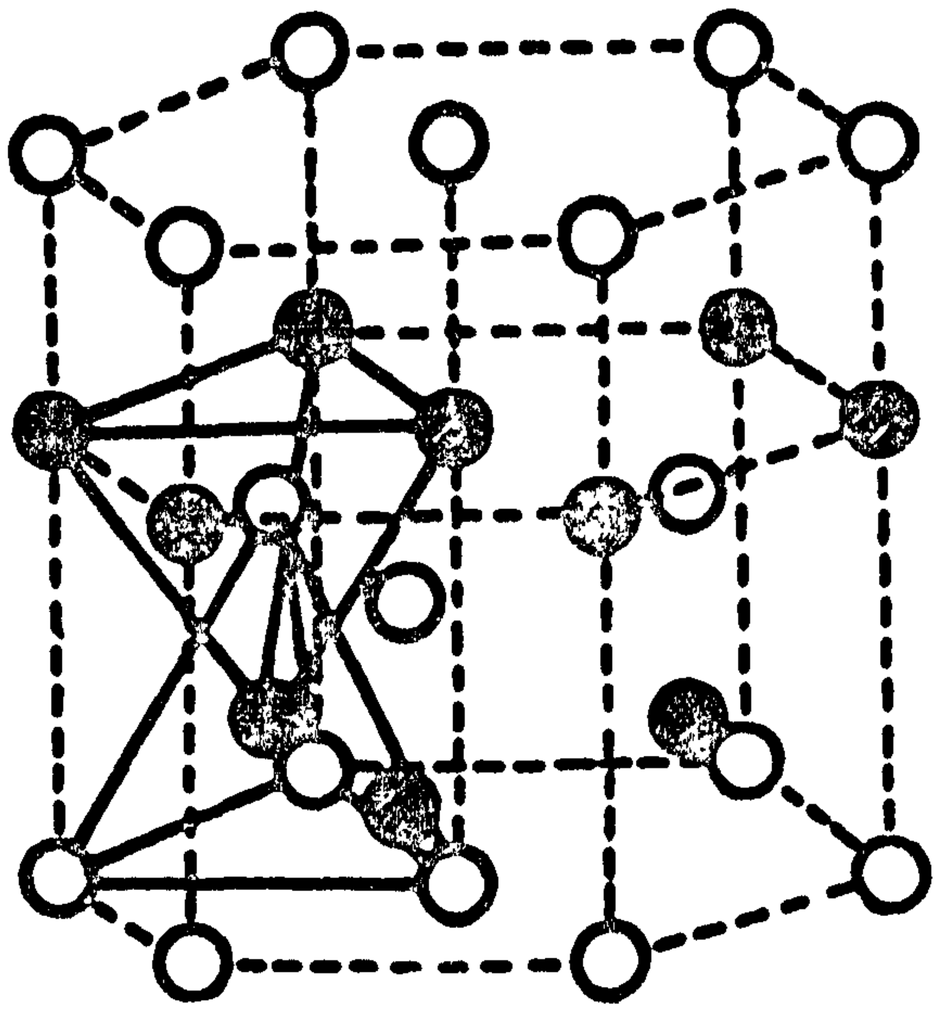


FIGURE 2.1a: Wurtzite Structure

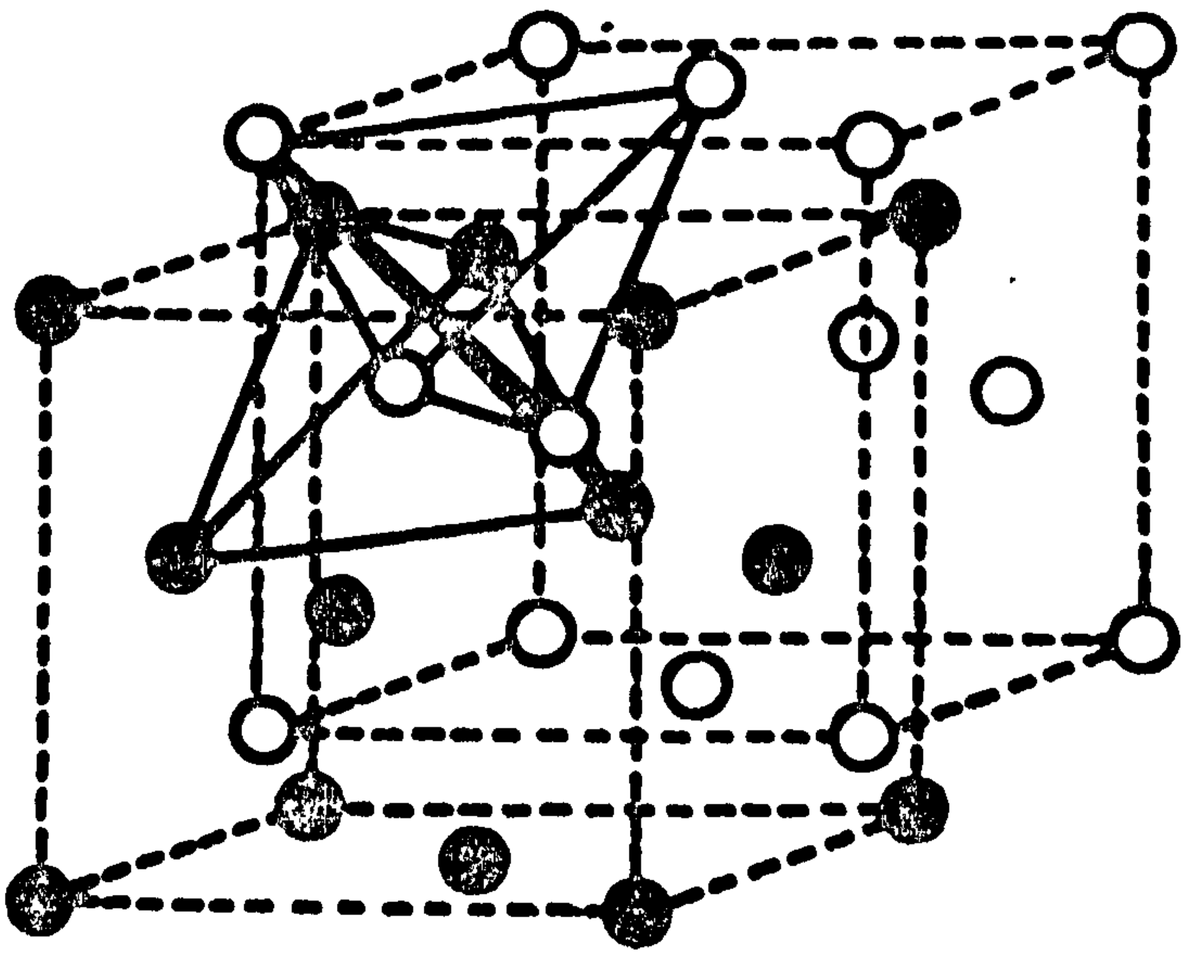


FIGURE 2.1b: Zinc Blende Structure

photoconductivity, a large piezoelectric effect, acoustoelectric amplification, luminescence (thermo-, photo-, tribo-, cathodo- and electroluminescence), laser emission, electrical conductivity storage, etc. The details are given in Refs. 36 and 37.

2.2.1 Impurity Doping in CdS

CdS is not amphoteric, and can only be made n-type. Any attempt to diffuse in acceptor impurities results in self compensation by vacancies to maintain charge neutrality. In its bulk form CdS has a very high resistivity. However, during growth it is easy to choose deposition conditions such that a sulphur deficiency is created. Non-stoichiometric CdS leads to self-doped conductivity. Impurity dopants such as the halogens (Cl, Br, I) and group III elements Al, In, Ga, can also be introduced into CdS to reduce the resistivity. This can be explained in the following way.

Suppose an impurity atom such as Cl with seven outer shell-electrons replaces S substitutionally. Since Cl requires one electron to complete its outer shell, there is one electron left over that will be weakly bound in the vicinity of the Cl imperfection at sufficiently low temperature. If we represent this by Cl^{*}_{s}, at higher temperature ionization takes place and $Cl^{*}_{s} \rightarrow Cl^{o}_{s} + e'$. Depending on the ambient conditions, for every two Cl atoms substituting for one S atom, a cadmium vacancy may be formed, when $2\ S^{*} + Cd^{*} + 2\ Cl \rightarrow 2\ Cl^{o} + V_{Cd}^{''} + 2\ S + Cd$. This can be written as $Cd^{*} + 2\ e \rightarrow V_{Cd}^{''} + Cd$. The cadmium vacancy has accepted two electrons from the chlorine impurities. An attractive Coulomb force can also associate these defects so that pairing between donors and acceptors takes place and a complex $(V_{Cd}Cl_{s})'$ is formed. Similar substitution process occurs if a Cd atom is replaced by a trivalent cation such as In. The neutrality conditions governing the substitution are $In_{Cd} = e'$ and $2\ In^{o}_{Cd} = V_{Cd}^{''}$.

These results can also be explained pictorially by considering the covalent model (Fig 2.2). Cd and S each make four bonds because of the tetrahedral arrangement of the structure in the sphalerite or wurtzite lattices. Each bond can be considered as effectively composed of $\frac{1}{2}$ an electron from the Cd and $1\frac{1}{2}$ electrons from the S. If Cd is replaced by In with three electrons available for bonding, only two are required and one is kept over to become a free electron at high temperature. Similarly if S is replaced by Cl with seven electrons, one electron is again in excess. If Cd is replaced by Cu, one more electron is required for bonding and this electron is taken from a neighbouring S, freeing a hole in the process. Thus in CdS, substitution of Cl, Br, I for sulphur and aluminium, gallium and indium for cadmium creates shallow donor levels while copper and silver produce acceptor levels. The alkali metals sodium, potassium and lithium provide shallow acceptors in CdS.

The characterisation of the localised levels introduced into the forbidden gap of pure or intentionally doped CdS samples and their identification with crystal imperfections has been the subject of considerable research. Several techniques such as thermally stimulated conductivity (TSC), photodecay, space charge limited current (SCLC) etc.[38,39] have been used to study these defects. More recently the techniques of admittance spectroscopy[40], transient capacitance measurement[41], photocapacitance[42,43], deep level transient spectroscopy (DLTS)[44,46], optical DLTS[47] have been used extensively to investigate the location and nature of these imperfections in the forbidden gap of CdS.

2.3 PREPARATION OF CdS

2.3.1 Single Crystals

Single crystals of CdS are frequently grown from the vapour phase because the compound sublimes at a lower temperature (700°C) under reduced pressure. Crystals are grown either by subliming the actual compound or by reacting the constituents in the vapour phase. Another method is to use a carrier

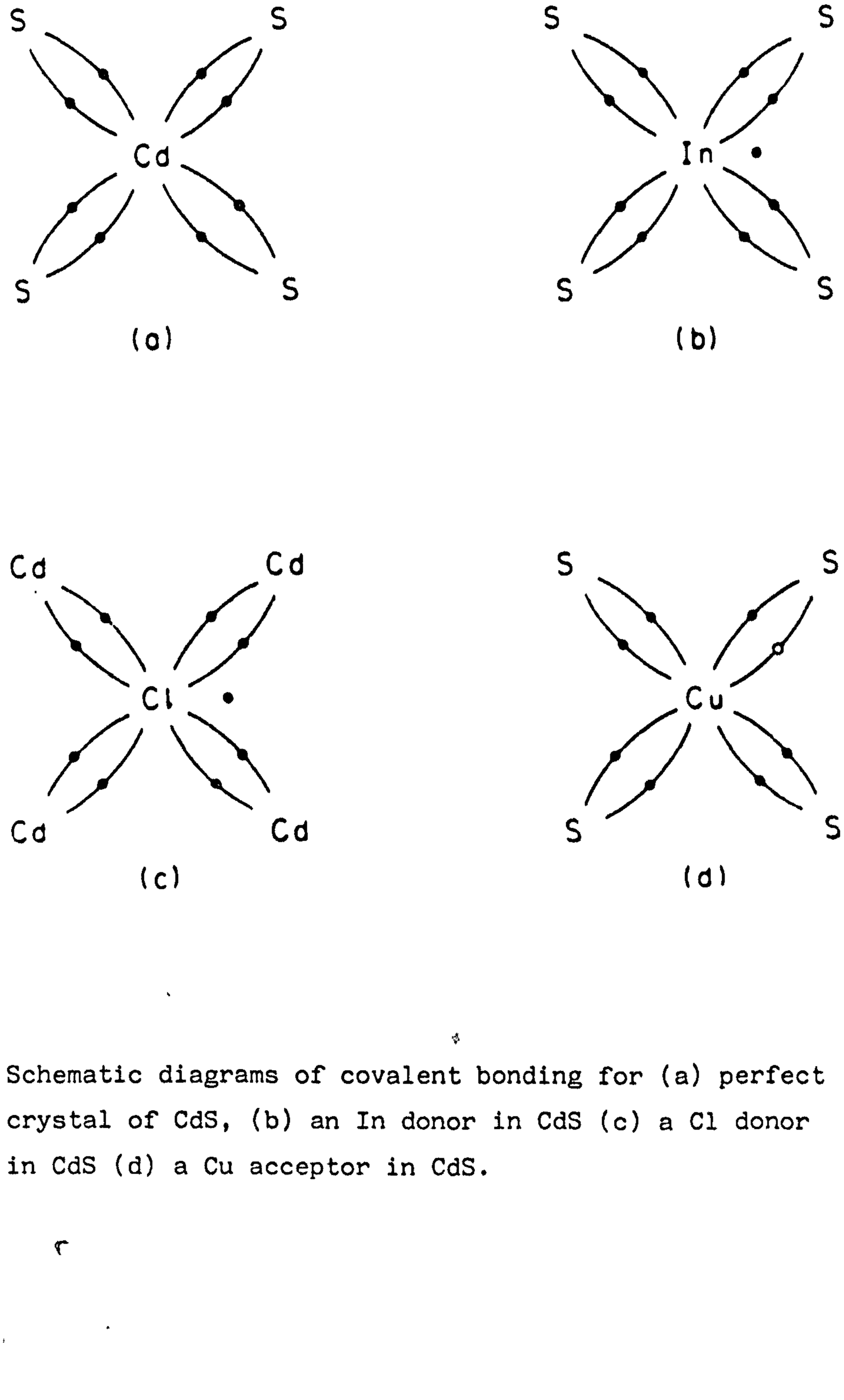


FIGURE 2.2: Schematic diagrams of covalent bonding for (a) perfect crystal of CdS, (b) an In donor in CdS (c) a Cl donor in CdS (d) a Cu acceptor in CdS.

gas to transport the constituents. The sublimation method was developed by Reynolds and Czyzack[48]. Piper and Polich[49] improved the technique and established a temperature gradient along the growth ampoule. Thus the material was transported from the hot to the cooler end of the tube. The growth ampoule was then moved relative to the furnace as the crystal grew. Clark and Woods[50] modified the system by placing the unsealed growth ampoule inside an argon filled furnace tube and allowing the two tubes to communicate via a narrow opening. This method employed horizontal furnaces which resulted in the practical difficulty of aligning the ampoule along the central axis of the growth tube. This gave rise to a non-uniform radial temperature gradient which led to uncontrolled growth. To solve the problem Clark and Woods[51] introduced a vertical system using sealed growth tubes. This method has been employed in growing the CdS crystals used in this programme of work. With this technique the addition of a reservoir allows an appropriate vapour pressure to be established over the evaporating charge.

The work on single crystals has enabled us to study and understand various physical processes which occur at the junction without introducing complications associated with polycrystallinity, grain boundaries and other defects characteristic of thin film substrates. However, single crystals are not suitable for large area solar cells and thin films of CdS are required.

2.3.2 Thermally Evaporated Films

This process involves sublimation of cadmium sulphide powder from a heated chamber (1000^{o}C) and condensation onto a substrate maintained at 200-250^{o}C. Sometimes a hot wall chimney is also used to maintain the stoichiometry of the film. Several designs of source cell have been tried and are described in detail by Stanley[31]. A graphite source bottle has been used by the Stuttgart group[18] and also at the Institute of Energy Conversion[19] to obtain an evaporation rate of 1-2 μ m min^{-1}. It is normally believed that CdS dissociates into its constituents as $CdS \rightarrow Cd(g) + \frac{1}{2} S_2(g)$

through a four step process[52]. CdS, first of all, dissociates into cadmium and sulphur on the surface as CdS (solid) → Cd(surface) + S(surface). The loosely bound cadmium atoms on the surface can evaporate directly Cd (surface) → Cd(gas) but the single sulphur atoms are more likely to associate as 2S(surface) → S_2(surface) and finally evaporate as S_2(surface (surface) → S_2(gas). The condensation is regarded as the reverse process to evaporation. The depositon is affected by, evaporation rate, source temperature, substrate temperature, and film thickness, together with the composition of the residual gas in the vacuum chamber and the surface finish and properties of the substrate[31]. A detailed discussion of the thermal evaporation of cadmium sulphide to produce large area solar cells has recently been given by Rocheleau et al[53].

When a CdS film is deposited from a beam which is perpendicular to a heated substrate, the layer develops the hexagonal wurtzite structure with a fibre axis orientation of microcrystallites. The films are polycrystalline with the individual c-axes roughly aligned perpendicular to the substrate surface. However, with filmsdeposited with the beam incident obliquely on the substrate, the c-axes of the crystallites tend to align themselves parallel to the vapour beam. The effect may be enhanced by increasing the deposition rate and is employed in making ultrasonic transducers[54]. Crystallite size is a function of both film thickness and deposition rate and may be as large as several microns for a 20 μm thick film[55,56].

The substrate temperature has a considerable influence on the structure of a film, since the cubic sphalerite modification is predominant at temperatures below 150°C [57]. As the temperature is raised the hexagonal content increases. With higher temperatures there are conflicting reports. Bujjatti[58] and Galkin et al[59] found a predominantly hexagonal structure for films deposited at 250°C but Shalimova et al[60] found an increasing cubic content at that temperature. As the substrate temperature is increased to 400°C, re-evaporation occurs and it is difficult to form a deposit[61].

It is generally accepted that the resistivity increases with increasing substrate temperature, but decreases with increasing evaporation rate. A variation in the dark resistivity as a function of film thickness has also been reported by Wilson and Woods[62] and Buckley and Woods[63]. The electron Hall mobility μ_H is also affected by the deposition conditions and typical values are of the order of 10 $cm^2\ V^{-1}\ sec^{-1}$. Photoluminescence effects have been observed in normally evaporated films[64] and also in thin films evaporated in an enclosed vacuum system[65].

Thermally evaporated films have been studied extensively and are the most successful to date for solar cell applications. A roll to roll coater has recently been reported for thermal deposition of CdS which can produce efficient cells[66]. Although thermal evaporation has been successfully used for depositing CdS films, the major disadvantage of the technique is that only a few percent of the material is used. Moreover the film has to be ~ 20 μm thick in order to avoid the problems of short circuiting through pinholes.

2.3.3 Sputter Deposited Films

With this technique vapour species are created by kinetic ejection from the surface of a material (the target) by bombardment with energetic and non-reactive ions. The ejection process, known as sputtering,takes place as a result of momentum transfer between the impinging ions and the atoms of the target surface. The sputtered atoms are condensed on a substrate to form a film. The simplest arrangement to produce ions is provided by a normal glow discharge created at a residual pressure of $\approx 10^{-2}$ torr in the required gas (generally argon), by applying 1 to 3 kV dc between a cathode and anode (on which the substrate is fixed). Other methods involve magnetron and r.f.sputtering[67]. Normally magnetron sputtering is used for the deposition of CdS layers[68]. In this system permanent magnets are placed behind the cathode in various geometries in such a way that the cathode surface has at least one region where the locus of the magnetic

field lines is parallel to the cathode surface in a closed path. This enhances the deposition rate. The ionization of the gas can also be enhanced with the help of an inductively coupled external r.f.field.

The chief advantage of sputtering is that over 80% of material can be used over large areas. However, the deposition rate is very slow and it is not easy to produce a low resistivity layer.

2.3.4 Films Produced by Spray Pyrolysis

CdS layers produced by this technique came very close to commercial production by Photon Power[69]. This procedure, initially suggested by Chamberlin and Skarman[70] and developed by Jordan[71] has been used in a pilot production line. With this method an aqueous solution of a cadmium salt and a sulphogenic compound is sprayed on to a heated substrate using the pressure provided by a compressed gas. The reaction which develops on the hot substrate produces a CdS layer and volatile products. With the commonly used $CdCl_2$ and thio urea, the reaction proceeds as follows.

$$CdCl_2 + SC(NH_2)_2 + 2H_2O \rightarrow CdS\downarrow + 2NH_4Cl + CO_2\uparrow$$

The spray process can be carried out in a N_2 atmosphere. The layers thus produced have the advantages of being more compact and stoichiometric than evaporated films so that their thickness may be reduced below 10 μm for use in photovoltaic devices. However, the disadvantage of this process is a slow deposition rate (few microns/hr). Recently, there have been improvements in this aspect in that Levart et al[72] have used airless spray technique to deposit CdS layers with faster growth rate.

2.3.5 Silk Screen Printed Layers

The earlier work of these thick films was concerned with the formation of sintered layers of photoconducting CdS powders[73]. Dopants such as chlorine and copper were sometimes used to increase the photosensitivity[74].

Ambient sensitive photoelectronic behaviour of CdS sintered layers has been reported by Micheletti and Mark[75]. Ceramic CdS substrates were used by Nakayama[76] to produce 6-9% efficient CdS/Cu_2S solar cells. Some work on indium doped pellets was also carried out at the Clevite Corporation but these were considered to consume too much material. Although silk screen printing has been used mainly for selective deposition of conductors and insulators[77,78], this technique using CdS ink for fabricating field effect transistors (Witt et al[79]) and large area photoconducting cells[80,81] has however been reported. Vodjani[83] made CdS/Cu_2S heterojunctions on a 20 μm thick silk screen printed films, however the efficiency of his cell was only 1%. Subsequently a major effort was made at the Wireless Research Laboratory, Japan, on the silk screen printing process for the formation of heterojunction devices.

The normal procedure which is adopted for silk screen printing includes the use of a high purity CdS powder which is first calcined in a silica boat in N_2 atmosphere and then crushed to produce a small grain size. The compound is spread with a suitable binder(propylene glycol or ethylene cellulose) and flux (normally $CdCl_2$). The particle size, viscosity, the pressure applied using the squeegee and mesh size of the screen affect the thickness and quality of the printed layer. Dopants such as Ga or In can be added at this stage of formation of the film. $CdSO_4$ has also been used to obtain conducting films. The films are dried and fired at a high temperature, 640-690°C, to promote sintering.8.5% efficient heterojunctions formed by electroplating a Cu_xS layer on the screen printed CdS have been reported by Matsumoto et al[83]. Silk screen printed CdS/CuIn Se_2 devices were fabricated by Garcia and Tomar[84]. Recently extensive work has been carried out on an all silk screen printed CdS/CdTe cell and efficiencies as high as 12.8% have been claimed[85].

The advantage of this process is that most of the material is fully utilized, although film thicknesses are of the order of 20-30 μm. Films

can readily be doped. The method is simple and can be employed without expensive equipment.

2.3.6 Electrophoretically Deposited Films

The process of electrophoresis for the deposition of CdS for solar cells has been used by Williams et al[86]. It involves the movement of colloidal particles of CdS by the application of an electric field, and their deposition onto a conductive substrate acting as an electrode. The sol is prepared by the precipitation of CdS from a reaction between a cadmium compound such as cadmium acetate and H_2S. With excess sulphur ions in the solution, a negative charge is developed on the colloidal particles. The effect of the electric field is to induce movement of the CdS particles through the sol and deposition takes place on the anode. The process produces a powder layer of tightly packed particles of about 100 Å diameter. Although the process is fast (deposition rate $\sim$ 2-3μm/min) and nearly all the material can be used,re-crystallization presents a major problem and thermal[97] and laser[88,89] annealing has been investigated.

All the methods described above for the production of thin and thick films of CdS have relative advantages and disadvantages which have been summarized by Hill and Williams[90]. A structure approaching that of a single crystal is ideal because the various polycrystalline films contain numerous grain boundaries, intergranular defects and electrically active impurities. Major problems are associated with the presence of grain boundary potential barriers and their effect on the series resistance of devices and the open circuit voltage. Problems of short circuit diffusion paths along grain boundaries can also prove disastrous.

The potential barriers at grain boundaries in CdS films have been investigated by many workers[91,92,93]. The interface tends to possess negative charge with a resultant accompanying narrow depletion region and a barrier height ranging from 0.015 to 0.2 eV[93]. The effect of such

barriers on the majority carrier mobility has been discussed by Petritz[94] who suggested that the mobility is an exponential function of temperature and barrier height according to the equation $\mu_H = \mu_o e^{-q\phi/kT}$. In order to minimize the effects of intergranular barriers, recrystallization of the films is desirable. The presence of Ag, Cu have been found to activate the process of recrystallization[95,96]. The effects of these dopants on the electrical properties of thermally evaporated films have been described by Dresner and Shallcross[97] who found a high mobility of 300 $cm^2 v^{-1} s^{-1}$ with a crystallite size of 10 μm.

2.4 COPPER SULPHIDE

2.4.1 General Properties

Since the Cu_xS is the absorber generator in the CdS/Cu_xS cell, the electrical and optical properties of this layer determine the light generated current. Copper sulphide is a complex material since copper can be either monovalent or divalent or can form salts in its normally divalent form with a copper deficient defect structure. As a result it is normally designated as Cu_xS. In between cupric sulphide, CuS (covellite) and cuprous sulphide, Cu_2S (chalcocite) there are three more stable phases[98] namely djurleite (x = 1.96), digenite (x = 1.8) and anilite (x= 1.75). The compositional region of interest for solar cells extends from chalcocite to djurleite. Chalcocite (x = 1.995-2.000) has a monoclinic structure[99], usually twinned to give an effectively orthorhombic structure at room temperature which transforms to hexagonal at 104°C. Djurleite has an orthorhombic structure at room temperature[100] transforming to tetragonal at 86-93°C and to cubic at 100°C. Digenite with a pseudo cubic structure at room temperature transforms to cubic at 78°C. The phase diagram of the Cu-S system between covellite and Cu_2S is shown in Fig 2.3. Cook et al[101] observed that a mixture of chalcocite and djurleite exists in the compositional range $1.96 < x < 1.98$ but the structure appears to be

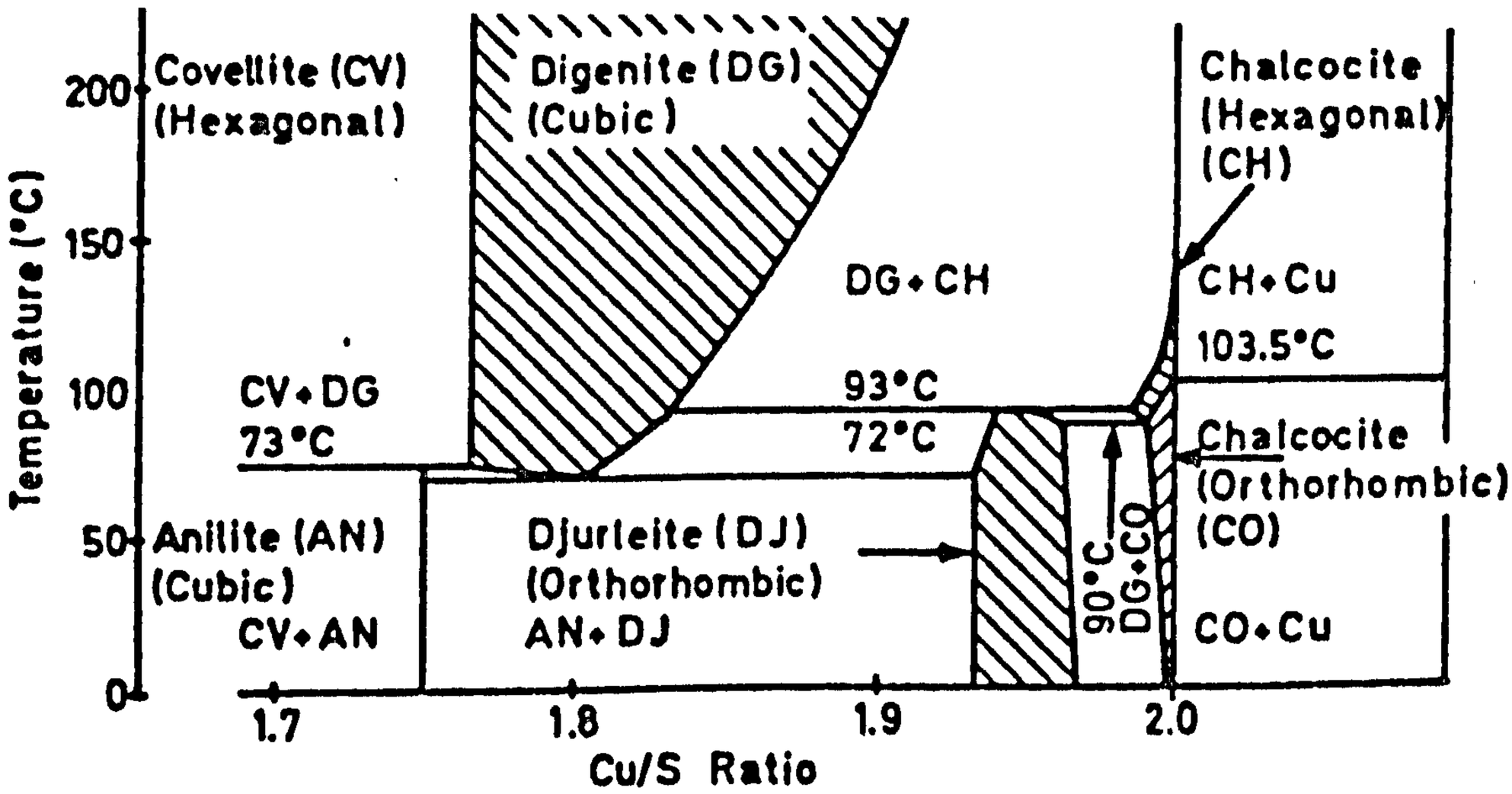


FIGURE 2.3: The Phase diagram of copper sulphides (Ref 98)

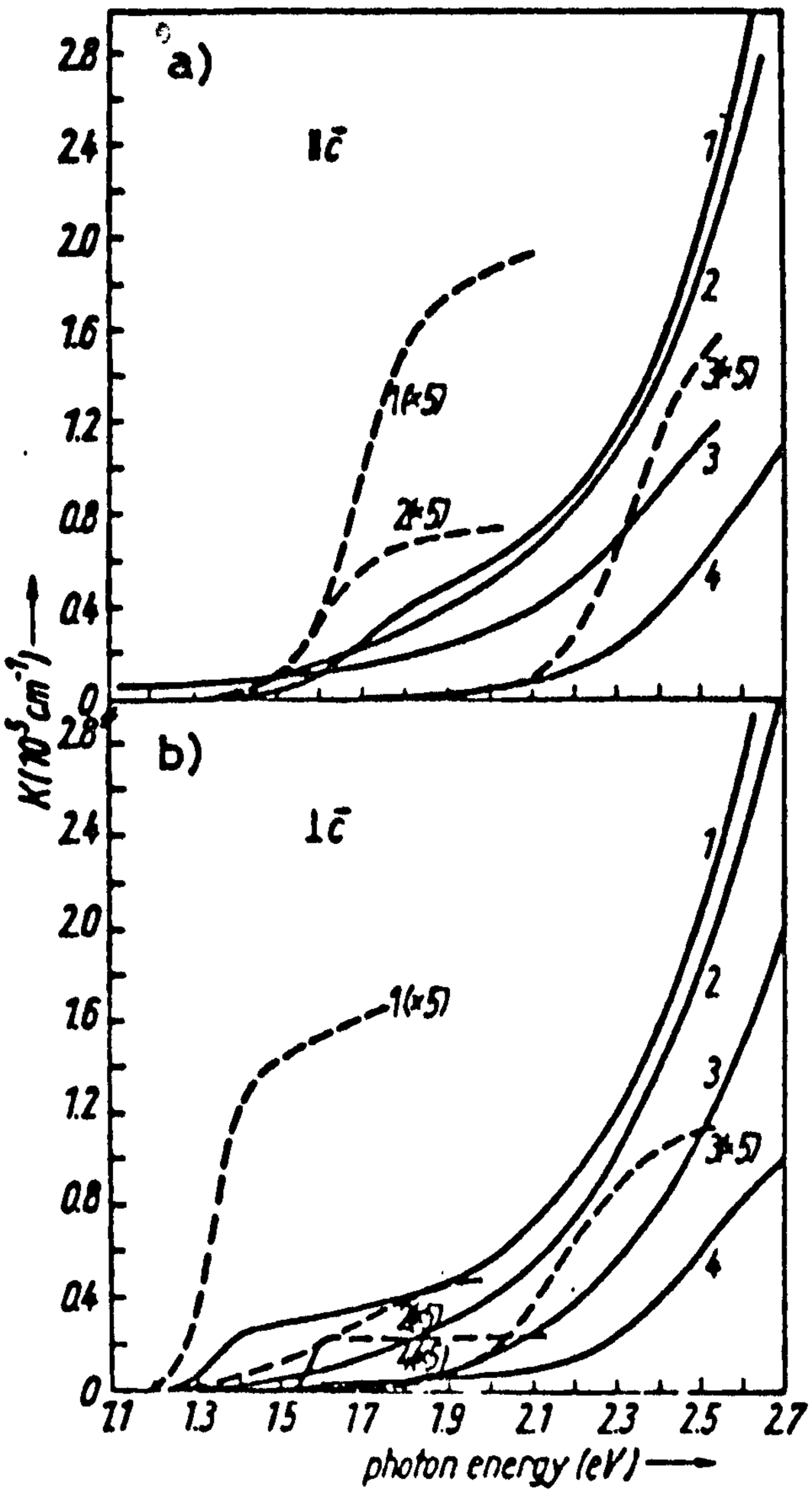


Fig 2.4: The energy dependence of the absorption coefficient (Ref 102) arising from interband transitions in Cu_xS

The light coming

(a) parallel,

(b) perpendicular to c-axis

—·—·— Sum of the direct and indirect bands

----- indirect band only

(1) chalcocite

(2) djurleite

(3) $Cu_{1.9}S$

(4) digenite

hexagonal in the compositional range 1.96 < x <1.8. They also demonstrated that the atomic arrangement in djurleite is quite well matched to that in chalcocite. The defect structure of Cu_xS usually consists of a highly ordered sulphur sublattice with copper atoms in disordered sites.

Of these different forms of Cu_xS chalcocite is the only one which has a large absorption coefficient in the photon energy region between 1.2 eV and 1.5 eV when the illumination is parallel to c-axis (Fig 2.4). However there are some conflicting reports regarding the nature of the bandgap. While Mulder[102], Marshall and Mitra[103] and others[16,104] considered the bandgap of chalcocite to be indirect at 1.2 eV and direct in the range from 1.5-2.2 eV[102,105], Loferski and Schewchun[106], Burton and Windawi[107] and Rothwarf and Windawi[108] explained their results in terms of a direct bandgap. Even so, the existence of one edge at 1.2 eV at 300K is generally accepted in Cu_2S.

The variation in bandgap with changes in stoichiometry has been attributed to a Moss-Burstein shift. With increasing copper deficiency, the semiconductor becomes degenerate and the Fermi level enters the valence band. This gives rise to the effective direct energy bandgap observed by Mulder[102], Rothwarf and Windawi[108] and Kantariya et al[109]. The increased hole density affects the electrical properties also. The electrical and optical properties of Cu_xS have been reviewed by Stanley[24], Hill[25] and Savelli and Bougnot[26]. Chalcocite is a p-type semiconductor in which copper vacancies produce shallow acceptors. Carrier densities usually range from 10^{18} to greater than 10^{21} cm^{-3}. Reported Hall mobilities are usually low : 3-30 $cm^2\ V^{-1}\ sec^{-1}$ for single crystals and 2-7 $cm^2\ V^{-1}\ sec^{-1}$ for thin films. Thus resistivities commonly range from 10^{-3} to $6x10^{-1}$ Ω-cm for undoped material and to over 10^3 Ω-cm for Cd compensated material. Minority carrier diffusion lengths in chalcocite range from less than 0.1 μm to 0.6 μm in thin films[110,111], but in djurleite values are smaller than 50 $\overset{o}{A}$ [112].

Considering these optical and electrical properties it is obvious that chalcocite is the desired phase of Cu_xS for solar cell applications. Te Velde and Dieleman[113] have demonstrated that the efficiency of a cell with chalcocite is about an order of magnitude higher than that of cell with djurleite. An even poorer response was obtained with $Cu_{1.8}S$. Palz et al[114] found a similar relationship between stoichiometry and photovoltaic response. Rothwarf[115] concluded that the maximum efficiency occurs with x very close to 2.0 and deviation from this value during the operating lifetime of a cell is accompanied by a degradation process.

2.4.2 Growth of Cu_xS

The most frequently used chemiplating process is that developed by the Clevite Corporation. The Cu_xS is grown via a topotaxial exchange reaction in which each of the Cd ions is replaced with two Cu ions while the sulphur sublayer remains intact. Boer[30] compares this formation of the Cu_xS layer on the upper part of each columnar grain with a tooth covered by its dental enamel. Normally CdS is dipped in a hot solution ($90^{o}C$) of CuCl. The exchange reaction takes place and Cu_2S is formed. The reaction can be described as $CdS + 2\ CuCl \rightarrow Cu_2S + CdCl_2$. The pH and concentration of the solution, dipping time and the temperature are the important factors which need to be carefully monitored[16]. The technique is very simple and widely employed. Its disadvantages are that the process is very fast and the problem of diffusion of copper down the grains causes severe problems of shunting paths in very thin films.

The electroplating process has been used for forming Cu_xS on ceramic CdS by Nakayama[76] and on silk screen printed CdS films by Matsumoto et al[85]. In this method the CdS layer and a copper plate are immersed in an aqueous $CuSO_4$ solution and a current is passed through the electrolyte via the two electrodes. The reaction proceeds as $Cu^{++} + CdS = CuS + Cd^{++}$ and $CuS + (x-1)Cu^{++} + 2(x-1)e = Cu_xS$[85]. The effects of varying the con-

centrations, pH and temperature of electrolyte on the stoichiometry of the Cu_xS have been reported in Ref.116. Cu_xS with the best stoichiometry was obtained using a temperature of 55-65^{o}C with a current density of 2.5-5 mA cm^{-2} while maintaining a 0.4 M concentration bath at a pH of 2.5.

Cu_xS films can be deposited by flash evaporation in vacuum. This procedure offers an opportunity of studying the properties of the Cu_xS layers separately. Vanderwal et al[117] reported 6% efficient cells obtained by this technique. The effects of the depositional parameters on the stoichiometry of the Cu_xS has also been investigated and layers with good stoichiometry have been produced[118,119]. Sputtering has also been used for this purpose. Layers of Cu_xS can be deposited using a $Cu_{1.98}S$ target and an atmosphere (2×10^{-2} m bar) consisting of a mixture of argon with a small amount of reactive gas (H_2 or H_2S). All sputter deposited Cu_2S/CdS junctions have been reported by Thorton and Anderson[68].

In the solid state reaction method, first proposed by Te Velde[11], freshly bleached CuCl is vacuum evaporated on to CdS, and the substrates are subsequently heated in an inert atmosphere at $\sim$ 200^{o}C for a few minutes. The solid state reaction is similar to the chemical exchange reaction and a layer of Cu_xS is formed topotaxially on CdS. The unwanted $CdCl_2$ is removed by rinsing in absolute alcohol. The process is shown diagramatically in Fig 2.5. The technique has the advantage that the reaction proceeds much more slowly than in the wet process and penetration down grain boundaries is limited[25]. The method is very useful therefore with very thin films. However the thickness of the Cu_xS is then limited[120]. Casperd and Hill[121] studied the process in detail and observed the inter-diffusion of Cu and Cd. They proposed that an impermeable layer of $CdCl_2$ is produced which inhibits the reaction after some time They also found that cells prepared using the dry barrier process had a better match to the air mass 1 spectrum than wet plated devices[122]. A comparison of wet plated and dry processed cells has also been made by Baron et al[123].

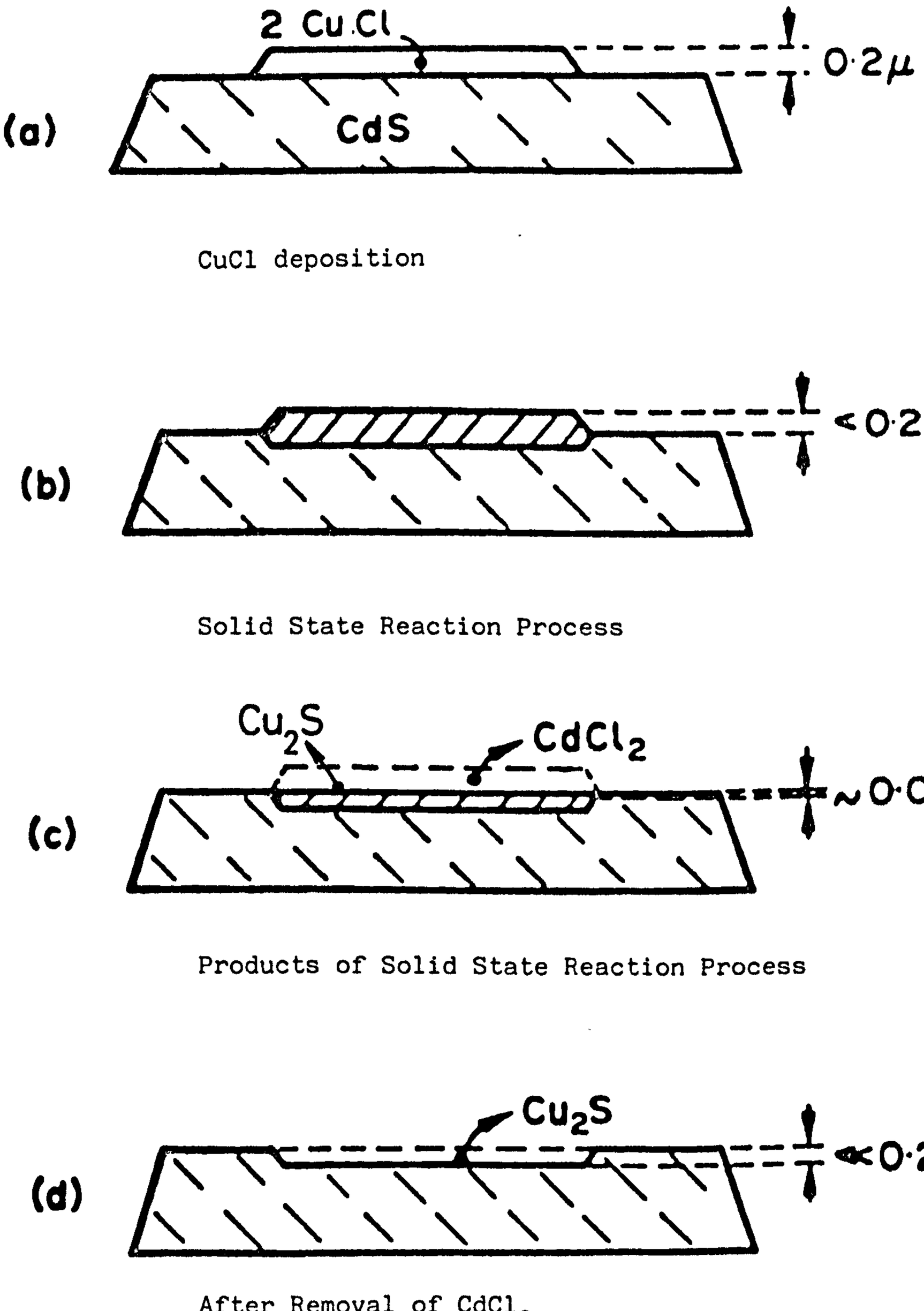


FIGURE 2.5: Schematic representation of the stages in the dry barrier process (Ref 11)

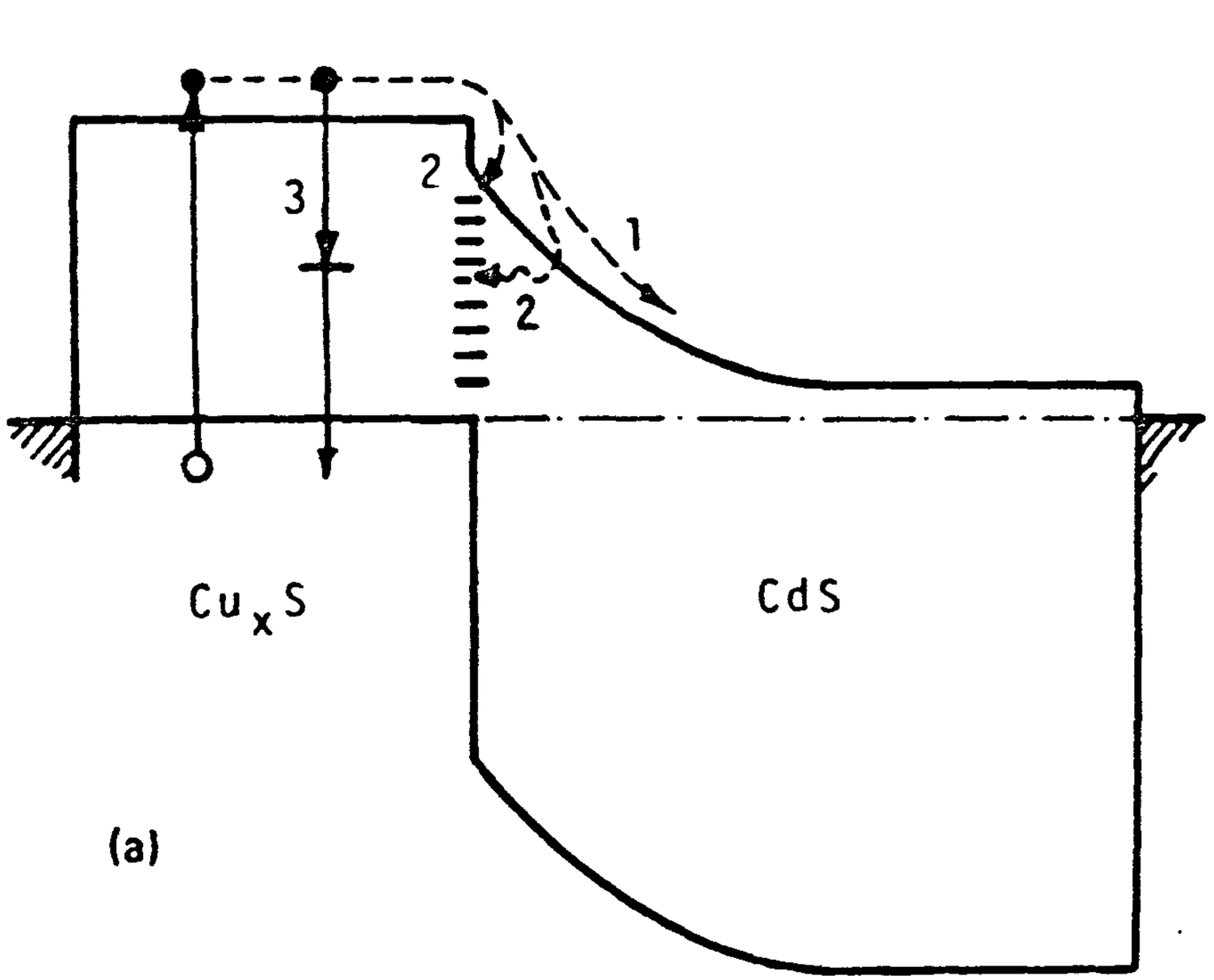
In conclusion it is usual for cells formed using each of the methods of Cu_xS formation described above to be given a short heat treatment at $\sim 200^{o}C$ in air, vacuum or inert atmosphere to complete the device fabrication process.

2.5 PHOTOVOLTAIC PROCESSES IN THE CdS/Cu_2S JUNCTION

Although the fabrication of the CdS/Cu_2S photovoltaic device is very simple, the junction is very complex as a result of interfacing two materials with different electron affinities, bandgaps and crystal structures. Lattice mismatch, and inter-diffusion of components during heat treatment introduces defect states at or near the interface that strongly affect the properties of the junction. In particular diffusion of copper into the CdS adjacent to the interface gives rise to cross-over effects between the current voltage characteristics measured in the dark and in the light, and complex photo effects associated with Cu doped CdS[27]. These include quenching of photocurrent by infrared illumination, an enhancement of SCC by blue light and large changes in capacitance values with A M 1 illumination[124]. Further the spectral response of the cell depends on its optical and thermal history, the presence of bias illumination and the temperature during which the actual measurements are made[110,124]. Its photovoltaic properties are also controlled by the phase of Cu_xS[27,113,114,125]. The junction has therefore sustained wide academic interest and many different models have been proposed.

According to Shiozawa et al[126], carrier transport is controlled by the series resistance of a photoconducting Cu doped i-layer adjacent to the junction which is formed by diffusion of Cu during the heat treatment. They proposed a discontinuous notch of 0.35 eV at the interface. Van Aerschodt et al[127] disputed the existence of an i-layer from their measurements of current voltage characteristics where they found a sharp rise in current at high forward bias. Gill and Bube[110] and Lindquist and Bube[128] assumed the presence of a spike at the CdS/Cu_xS interface due to differences in the

electron affinity. They concluded from studies of the optical quenching of photocurrent and photocapacitance that the width of the spike was controlled by the trapped charge near the interface, which modulates the transparency of the spike to photoexcited electrons diffusing from the Cu_2S. The transport of photogenerated carriers was thought to be controlled by tunnelling through the spike or by thermal excitation over it. The height of the spike was estimated to be between 13 and 60 meV. However, there is no experimental evidence to suggest that a barrier voltage greater than the Cu_2S bandgap of 1.2 eV can be obtained. Considering the temperature dependence of the dark current voltage characteristics and capacitance measurements Fahrenbruch and Bube[124] next suggested a negative discontinuity in the conduction band at the interface, rather than a spike. They concluded that the electric field at the interface modulated the photogenerated carrier loss there due to tunnelling/recombination pathways through states in the interface regions (Fig 2.6). Te Velde[129] also considered a notch instead of a spike at the interface and explained the current voltage characteristics in terms of the height of the discontinuity which varied through the adsorption of oxygen at the interface as heat treatment in air proceeded. However, he did not consider the presence of copper in the depletion region and hence the various effects which depend in the wavelength of the incident illumination could not be explained. Nevertheless, Te Velde introduced recombination as a loss mechanism. In contrast Martinuzzi[130,131] made dark current voltage measurements and proposed a multistep tunnelling mechanism as the dominant feature in transport across the junction. Haines and Bube[132] suggested that a deep donor level with an ionization energy at 0.45 eV was responsible for increased tunnelling currents and interfacial recombination which in turn affected the device parameters. Boer[29] demonstrated the effect of donors on the shape of the current voltage characteristics. Earlier he proposed a different model in which high field domains were found in the CdS:Cu layer and these reduced the OCV but had little influence on SCC[133].



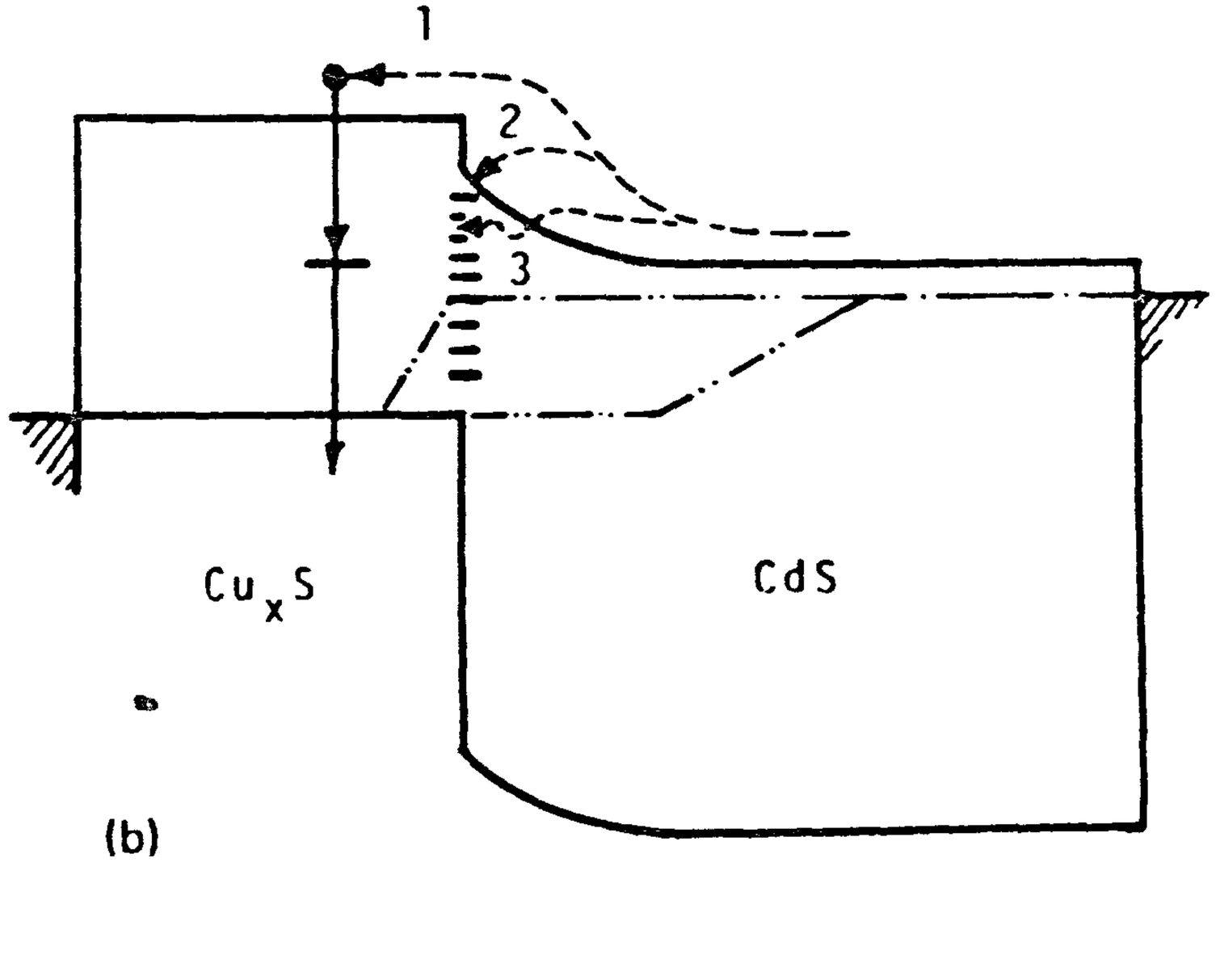


FIGURE 2.6: Energy band diagrams proposed by Fahrenbruch and Bube (Ref 31)

(a) Mechanism controlling the short circuit current : (1 collection by the junction field ; 2 recombination via interface states, possibly involving tunnelling steps, and 3, bulk and surface recombination).

(b) Mechanisms controlling the forward bias diode current (1 thermal excitation over the total barrier height, 2 thermally excited recombination through interface states ; and 3 tunnelling/recombination through interface states).

Further he suggested that increased recombination was attributable to donor-acceptor pairs formed in a half cylinder around each dislocation produced by lattice mismatch[30]. On the other hand, Partain et al[134] have suggested a space charge limited current theory to explain the CdS/Cu_2S heterojunctions.

A more comprehensive and well accepted model was proposed by Rothwarf[135] after a series of experiments at the Institute of Energy Conversion, Delaware. This model, illustrated in Fig 2.7, primarily describes the transport in terms of interfacial recombination which controls the electric field. The model assumes that (i) the stoichiometry of Cu_xS controls the carrier density and relative band bending in the two materials (ii) the CdS has shallow donors (because of excess Cd or intentional dopants) and deep levels (may be native or created by heat treatment), (iii), a 4% lattice mismatch between Cu_2S and CdS which creates a large density of interface states (about 10^{13} cm^{-2}) at the junction and (iv) the electron affinity of CdS exceeds that of the Cu_2S by $\Delta E_c = \Delta\chi$. The resultant model explains most of the observed results[27].

Recently Fahrenbruch and Bube[31] have summarised the behaviour of CdS/Cu_xS cells in a unified approach as follows (1) the optically active region for photogeneration of carriers is Cu_xS,(2) the electrons photoexcited in the Cu_xS are injected into the CdS for collection,(3) under operating conditions the forward bias current flows through the junction by recombination and/or tunnelling via interface states rather than over the barrier into the conduction band of the Cu_xS, (4) diffusion of Cu into the CdS occurs during heat treatment and widens the depletion region on the CdS side by compensation of CdS donors, (5) the low energy photon response is enhanced by high energy photon illumination because of the effects on the junction width, (6) dark and light forward bias J-V curves commonly cross in the heat treated cell and (7) long term loss of sensitivity is caused by changes in the composition

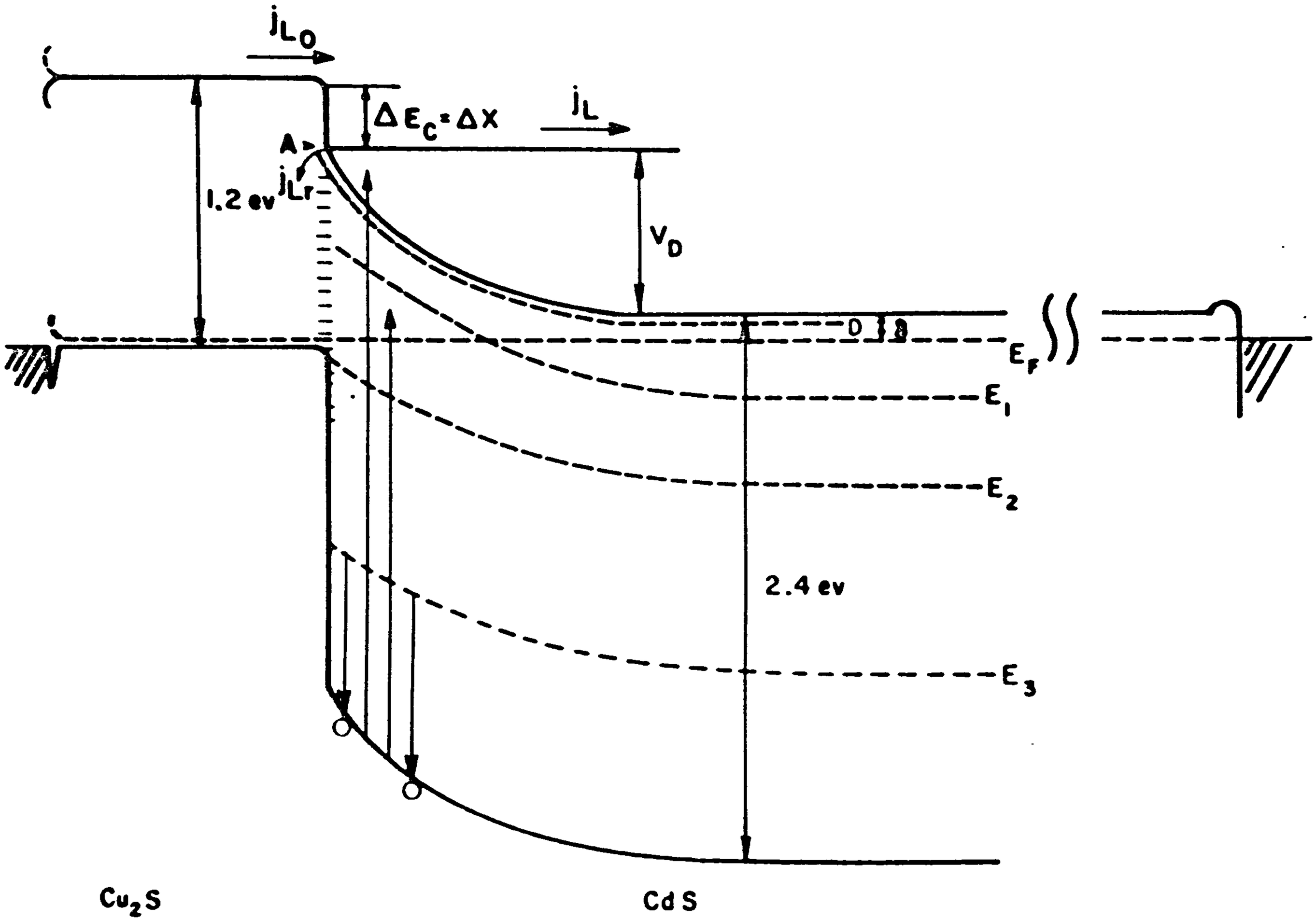


FIGURE 2.7: Energy band diagram, proposed by Rothwarf (Ref 27)

of the Cu_xS or, sometimes by additional diffusion of Cu into CdS.

2.6 $Cd_{1-y}Zn_yS/Cu_2S$ CELLS

The use of $Cd_{1-y}Zn_yS$ to improve the performance of CdS-Cu_xS cells was proposed[136] on the assumption that the lattice parameter and electron affinity of the solid solution can be matched to those of Cu_2S by varying the composition. The lattice parameters and electron affinities of CdS, ZnS and Cu_2S are shown in Table 2.1.

TABLE 2.1: Key Parameters for CdS, ZnS and Cu_2S (Ref. 138).

Parameters	CdS	ZnS	Cu_2S
Energy Gap Eg(eV)	2.42	3.58	1.20
Lattice Constant a(Å)	4.137	3.814	3.96
Electron Affinity χ(eV)	4.5	3.9-4.5	∿ 4.3

Clearly the mismatched electron affinities and lattice parameters can be reduced by replacing the CdS with $Cd_{1-y}Zn_yS$ alloy.

CdS and ZnS in the wurtzite modification have unit cells with volumes in the ratio ∿ 1.26/1 and cation radii with a ratio Cd^{++}/Zn^{++} ∿ 1.3. They are both n-type photoconductors and their reflectivity spectra show similar structures. In addition, native or intrinsic defects play a critical role in determining the electrical and luminescence properties of both materials[36,37].

Davis and Lind[138] showed that the growth of (CdZn)S single crystals by iodine vapour transport yields a highly uniform and relatively strain free single crystal of $Cd_{1-y}Zn_yS$ with a hexagonal structure. Similar mixed (CdZn)S crystals have been grown from the vapour phase in this laboratory using a modification of the method described by Clark and Woods[51]. Lattice parameters of (CdZn)S alloys have been studied by Ballentyne and Ray[139] and they showed that the c-axis dimension of the wurtzite structure of alloys

decreases sublinearly with zinc content. The optical bandgap of the CdS-ZnS system exhibits a monotonic but non-linear increase with increasing zinc composition.

Several techniques have been used to form thin films of $Cd_{1-y}Zn_yS$ e.g. thermal evaporation, spray pyrolysis and sputtering. The simplest way is to evaporate from a ternary powder, however a large compositional gradient is usually observed due to preferential evaporation of cadmium[140]. The technique which has been found to yield uniform films is to evaporate CdS and ZnS placed in two concentric cylindrical cavities placed into single graphite crucibles[141]. The other promising method has been spray pyrolysis[142,143].

Heterojunctions have been prepared both by wet plating and dry barrier techniques and have been reviewed by Burton[131]. The highest efficiency reported so far for $Cd_{1-y}Zn_yS/Cu_xS$ cells is 10.2%. The junction model is basically the same as that for CdS/Cu_2S but modified to allow for the change in the band parameters of the $Cd_{1-y}Zn_yS$.

REFERENCES TO CHAPTER 2

1. D.C. Reynolds, G.Leies, L.L.Antes and R.A.Marburger, Phys.Rev. 96 (1954) p.533.
2. J.Woods and J.A.Champion, J.Electron Control. 7 (1960), p.243.
3. R.Williams and R.H.Bube, J.Appl.Phys. 31 (1960), p.968.
4. E. D. Fabricius J.Appl.Phys. 33 (1962), p.1597.
5. H.G.Grimmeiss and R.Memming, J.Appl.Phys. 33 (1962) p.2217.
6. N.Duc.Cuong and J.Blair, J.Appl.Phys. 37 (1966) p.1660.
7. D.A.Cusano, Solid State Electron. 6 (1963), p.217.
8. E.R.Hill and B.G.Kermidas, IEEE Trans.Electron.Devices, ED-14 (1967),p 22.
9. B.Selle, W.Ludwig and R.Mach, Phys.Status Solidi 24 (1967), K145.
10. A.E.Potter, and R.L.Schalla, NASA.Techn.Note.NASATN D-3849, Washington, D.C. (1967).
11. T.S. Te Velde, Energy Conversion, 14 (1975), p.111.
12. G. Nadjakov, R. Andreitchine and M.Borissov; IZV Bulg.Akad.Nauk, 4 (1954), p.10.
13. F.Cabannes, C.R.Acad.Sci. 246 (1958), p.257.
14. H.Moss: Proc.Nat.Aeronaut. Electron Conf.1960, p.47.
15. F. A.Shirland: Advanced Energy Conversion 6 (1966) p.201.
16. L.R.Shiozawa, F.Augustine, G.Sullivan, J.M.Smith, and W.R.Cook, Clevite Corp.Final Report (Airforce Contract AF33(615)-5224) Aerosp.Res.Lab., Ohio, 1969.
17. A. Rothwarf and A.M.Barnett, IEEE Trans.Electron Devices ED:24 (1977)p.381.
18. R.B.Hall and J.D.Meakin, Thin Solid Films, 63 (1979) p.203.
19. R.W.Birkmire,R.B.Hall, J.E.Phillips and J.D.Meakin, 'Cadmium Sulphide/copper sulphide heterojunction cell research' final Report - Vol.I & II Sept.1979-1982. Sub contract XS-9-8309-1, Inst. of Energy Conversion, Univ.of Delaware.(Feb.1983).

20. H. W. Schock, G. Bilger, W.H.Bloss, G.H.Hewig and F.Pfisterer, Vacuum 27 (1977) p.281.

21. F. Pfisterer, H.W.Schock and G.H.Hewig, Proc. 2nd E.C.Photovoltaic Solar Energy Conf. Berlin (D.Reidel Pub.Dordrecht, 1979), p.352.

22. F.Pfisterer, H.W.Schock and J.Worner, Proc.3rd E.C.Photovoltaic Sol.Energy Conf. Cannes (D.Reidel Publ.Dordrecht 1980), p.762.

23. W.H.Bloss and F.Pfisterer: Proc.5th EC.P.S.E.C, Athens, Greece (D.Reidel Publ.1983), p.728.

24. A.G.Stanley, 'CdS solar cells' in Appl.Solid State Science, Vol.5. Ed.by R.Wolfe (Academic Press, 1975) p.251-366.

25. R.Hill, 'Thin Film Solar Cells' in Active and Passive Thin Film Devices , Ed.T.J.Coutts (Academic Press, 1978) p.487.

26. M. Savelli and J.Bougnot, 'Problems of the Cu_2S/CdS Cells' in Topic in Applied Physics. Solar Energy Conversion. Vol.31. Ed. B.O.Seraphin, (Springer-Verlag, Berlin, and New York,1979) p.213.

27. A.Rothwarf, Solar Cells, 2 (1980), p.115.

28. S. Martinuzzi, Solar Cells 5 (1982) p.243.

29. K.W.Boer, Phys.Stat.Sol. (a) 66 (1981) p.11.

30. K.W.Boer, J.Crystal Growth, 59 (1982) p.111.

31. A.L.Fahrenbruch and R.H.Bube, 'Fundamentals of Solar Cells', Photovoltaic Solar Energy Conversion (Academic Press,New York,1983).

32. K.L.Chopra and I.H.Khan, Surf.Sci 6 (1967) p.33.

33. D.M.Wilcox and D.B.Holt, J.Mat.Sci. 4 (1969) p.672.

34. H.Holloway and E.Wilkes, J.Appl.Phys. 39 (1968) p.5807.

35. W.E.Mecalf and R.H.Fahrig, J.Electro.Chem.Soc. 105 (1958) p.719.

36. M.Aven and J.A.Prenner: Physics and Chemistry of II-VI Compounds' (North Holland, 1967).

37. B.Ray, 'II-VI Compounds' (Pergamon Press, 1969).

38. J.Woods and K.H.Nicholas, Brit.J.Appl.Phys. 15 (1964) p.1361.

39. M.A.Carter and J.Woods, J.Phys. D 6 (1973) p.337.

40. A.Kobayashi, J.Appl.Phys. 49 (1978) p.934.

41. J.Oualid, D.Sarti, J.Gervais,& S.Martinuzzi, J.Phys.C (Solid State Physics) 12 (1979) p.2113.

42. T. Suda and S.Kurita, J.Appl.Phys. 50 (No.1) (1979) p.484.

43. H.G.Grimmeiss, N.Kullendorf and R.Broser, J.Appl.Phys. 52 (1981)p.3405.

44. C. Grill, G.Bastide, G.Sagnes and M.Rouzeyre: J.Appl.Phys. 50 (1979) p.1375.

45. P.Besomi and B.Wessels, J.appl.Phys. 51 No.8 (1980), p.4305.

46. M.Hussein, G.Lletti, G.Sagnes, G.Bastide, M.Rouzeyre: J.Appl.Phys. 52 No.1 (1981) p.261.

47. F.Poulin, A.W.Brinkman and J.Woods, J.Crystal Growth 59 (1982) p.240.

48. D.C.Reynolds and S.J.Czyzach, Phys.Rev. 96 (1959) p.1704.

49. W.W.Piper and S.J.Polich, J.Appl.Phys. 32 (1961)p.1278.

50. L.Clark and J.Woods, J.Cryst.Growth 17 (1966) p.319.

51. L.Clark and J.Woods, J.Cryst.Growth 3 (1968) p.126.

52. G.A.Somorjai and D.W.Jepson, J.Chem.Phys. 41 (1964), p.1389.

53. R.E.Rocheleau, B.N.Baron and T.W.F.Russell, Alch E.Journal 28 (1982) p.656.

54. S. Fukunishi and N.Niizeki, Jap.J.Appl.Phys. 8 (1969) p.1274.

55. R.R.Addiss, Trans.10th Nat.Vac.Symp.(Macmillan,1963) p.354.

56. F.V.Shallcross, R.C.A.Rev. 28 (1967), p.569.

57. J.F.Hall and W.F.C.Ferguson, J.Opt.Soc.Am.45 (1955) p.714.

58. M.Bujatti, Brit.Journ.Appl.Phys. 1 (1968) p.983.

59. B.D.Galkin et al, Sov.Phys.Crystallog. 12 (1968) p.766.

60. K.V.Shalimova, A.F.Andrushko, V.A.Dmitriev and L.P.Pavlov, Soviet Phys.Crystallography, 9 (1964), p.340.

61. P.H.Wendlend, J.Opt.Soc.Amer.52 (1962), p.581.

62. J.I.B.Wilson and J.Woods, J.Phys. Chem.Solids 34 (1973) p.171.

63. R.W.Buckley and J.Woods, J.Phys.D.Appl.Phys. 7 (1973) p.197.

64. W.P.Bleha and R.N.Peacock, J.Appl.Phys. 41 (1970), p.4992.

65. R.W.Buckley and J.Woods, J.Phys.D: Appl.Phys. 7 (1974) p.663.

66. T.W.F.Russell, R.E.Roucheleau, D.J.Lutz, D.F.Brestovansky and B.N.Baron, Proc.16th IEEE Photovoltaic Spec.Conf. (IEEE New York, 1982), p.743.

67. J.Comas and C.B.Cooper, J.Appl.Phys. 37 (1966) p.2820.

68. J.A.Thorton and W.W.Anderson, Appl.Phys. Lett. 40 (1982) p.622.

69. G.A.Roderick, Proc.3rd E.C.P.V.S.E.Conf.Cannes, Oct. 1980, (D.Reidel, Dordrecht, 1981) p.327.

70. R.R.Chamberlin and J.S.Skarman, J.Electrochem Soc. 113 (1966) p.86.

71. J.F.Jordon, Proc.Int.Conf.on Photovoltaic Power Generation, Hamburg, (1974) p.221.

72. M.Levart, B.Thiebaut and J.Vedel, Int.J.Solar Energy 1 (1983)p.1.

73. S.M.Thomson and R.H.Bube, Rev.Sci.Instrum.26 (1955) p.666.

74. M.J.B.Thomas and E.J.Zdanuk, J.Electrochem.Soc. 106 (1959) p.964.

75. F.B.Micheletti and P.Mark, J.Appl.Phys. 34 (1968) p.5274.

76. N.Nakayama: Jap.J.Appl.Phys. 8 (1969) p.450.

77. A.Nakano, H.Matsumoto, N.Nakayama and S.Ikegami, Jap.J.Appl.Phys. 19 (1980), p.157.

78. K.Firor and S.Hogan, Solar Cells 5 (1981-82) p.87.

79. W.Witt, F.Huber and W.Laznovsky, Proc.IEEE 54 (1966) p.897.

80. F.H.Nicoll and B.Kazan, J.Opt.Soc. A. 45 (1955) p.647.

81. D.P.Amalnerkar, M.S.Setty, N.R.Pavaskar and A.P.B.Sinha : Bull Matter. Sc. 2 (1980), p.251.

82. S.Vodjani, Electronics Lett. 9 (1973) p.128.

83. H.Matsumoto, N.Nakayama and S.Ikegami, Jap.J.Appl.Phys. 19 (1980),p.179.

84. F.J.Garcia and M.S.Tomar, Jap.J.Appl.Phys. 22 (1983) p.535.

85. H.Matsumoto, K.Kuribayashi, H.Uda, Y.Komatsu, A.Nakano, and S. Ikegami ; Solar Cells 11 (1984) p.367.

86. E.W.Williams, K.Jones, A.J.Griffiths, D.J.Roughley, J.M.Bell, J.H.Steven, M.J.Huson, M.Rhodes and T.Costich ; Solar Cells 1 (1979/80), p.357.

87. G.J.Russell, P.C.Pande, J.Woods, I.D.McInally and S.P.Gibbons, I.O.P. Conf.Ser.No. 67 (1983) p.189.

88. T.J.Cumberbatch, I.D.McInally and S.P.Gibbons, I.O.P. Conf.Ser. No. 67 (1983) p.195.

89. G.Martinez, J.L.Martinez and A. Zehe: Appl.Phys. Lett. 40 (1982) p.1031.

90. R.Hill and E.W.Williams, U.K.I.S.E.S. Conf.Proc(C-30) 'Photovoltaics a new Industry for Britain', (1982) p.1.

91. A.Rothwarf,Conf. Rec.12th IEEE Photovoltaic Specialists Conf. (Baton Rouge, L.A.), Nov.1976, p.488.

92. L.L.Kazmerski, W.B.Berry and C.W.Allen,8th PVSC (1980), p.9.

93. J.W.Orton, B.J.Goldsmith, M.J.Powell and J.A.Chapman, Appl.Phys. Lett. 37 (1980), p.557.

94. R.L.Petritz, Phys.Rev. 104 (1956) p.1508.

95. J.M.Gilles and J.Van Cakenberghe, Nature (London) 182 (1958) p.862.

96. A.Vecht and A.Apling, Phys.Stat.Sol. 3 (1963) p.1238.

97. J.Dresner and F.V.Shallcross, J.Appl.Phys. 34 No.8 (1962) p.2390.

98. R.W.Potter, J.Econ.Geol. 72 (1977) p.1524.

99. H.T.Evans, Nature (Phys.Science) 232 (1971) p.69.

100. S. Djurle: Acta Chem.Scand. 12 (1958) p.1415.

101. W.R.Cook, Jr., L.R.Shiozawa, F.Augustine, J.Appl.Phys. 41 No.7 (1970), p.3058.

102. B.J.Mulder, Phys.Stat.Sol. (a), 18 (1973) p.633.

103. R.Marshall and S.S.Mitra, J.Appl.Phys. 36 (1965) p.3882.

104. L. Eisenmann, Ann.Phys. (Leipzig) 6 No.10 (1952) p.129.

105. M.Ramoin, J.P.Sorbier, J.F.Bretzner and S.Martinuzzi, C.R.Acad. Science 268 (1969) p.268.

106. J .J.Loferski and J.Shewchun : Int.Workshop on CdS Solar Cells and other Abrupt Heterojunctions, (New York, Delaware, U.S.A. May 1975), p.318.

107. L.C.Burton and H.Windawi : J.Appl.Phys. 47 (1976) p.7621.

108. A.Rothwarf and H.Windawi: IEEE Trans.Electron Dev. ED-28 No.21 (1981). p.64.

109. R.V.Kantariya S. Yu Pavelets and G.A.Fedorus: Sov.Phys.Semicond. 13 (1979) p.693.

110. W.D.Gill and R.H.Bube, J.Appl.Phys. 41 (1970), p.3731.

111. L.Partain, J.H.Oakes, I.G.Greenfield, Int.Workshop on CdS Solar Cells and other Abrupt Heterojunctions, Univer. of Delaware, New York, (1975) p.346.

112. B.J.Mulder, Phys. Stat.Sol (a) 13 (1972) p.569.

113. T.S.Te Velde and J.Dieleman : Philips Res.Rep.28 (1973) p.573.

114. W.Palz, J.Besson, T.Nguyen Duy, and J.Vedel: Proc. 9th IEEE Photovoltaic Specialists Conf. (1972) p.91.

115. A.Rothwarf, Proc.2nd E.C.Photovoltaic Sol.Energy Conf.Berlin: (D.Reidel Pub.Dordrecht, 1979) p.370.

116. S. Saksena, D.K.Pandya and K.L.Chopra: Thin Solid Films, 94 (1982) p.223.

117. T.Vanderwel, R.Clarke, F.Scholz, D.Burk, N.Dalacu, and J.Shewchun, Proc.14th IEEE Photovoltaic Specialists Conf. (1980) p.694.

118. B.Selle and J.Megge: Phys.Status Solidi 30 (1968) K.153.

119. A.C.Rastogi, S.Salkalachen and V.G.Bhide: Thin Solid Films 52 (1978) p.1.

120. J.Dieleman, Proc.Int.Workshop on CdS Solar Cells and other Abrupt Heterojunctions, Delaware, (1975) p.92.

121. A.N.Casperd and R.Hill : Proc.Photovoltaic Solar Energy Conference, Luxembourg, (1977) p.1131.

122. A.N.Casperd and R.Hill: Solar Cells 1 (1979/80) p.347.

123. B.Baron, A.W.Catalano and E.A.Fagen: Proc.13th IEEE Photovoltaic Specialists Conf.Washington D.C. (1978) p.406.

124. A.L.Fahrenbruch and R.H.Bube: J.Appl.Phys. 45 (1974) p.1264.

125. P.Mascicott: Phys.Status Solidi (a) 11 (1972) p.531.

126. L.R.Shiozawa, G.A.Sullivan and F.Augustine, Proc.7th PVSC. Nov.1968, Pasadena, U.S.A. (IEEE New York, 1968) p.39.

127. A.E.Aershodt, J.J.Capart, K.H.David, M.Fabbricotti, K.H.Heffels, J.J.Loferski, and K.K.Reinhartz, IEEE Trans. Electron Devices 18 (1971) p.471.

128. P.F.Lindquist and R.H.Bube: J.Appl.Phys. 43 (1972) p.2839.

129. T.S.Te Velde: Solid State Electronics 16 (1973) p.1305.

130. S.Martinuzzi and O.Mallem: Phys.Stat.Sol (a) 16 (1973) p.339.

131. S.Martinuzzi, O.Mallem and T.Cabot: Phys.Stat.Sol(a) 36 (1976)p.227.

132. W.G.Haines and R.H.Bube: IEEE Trans.on Elect.Devices E.27 (11) (1980), p.2133.

133. K.W.Boer: Phys.Rev. B 13 (1976) p.5373.

134. L.D.Partain, G.A.Armantrout, J.Leong,P.Warter: J. of Elect. Mat. 9 (1980), p.467.

135. A.Rothwarf, Proc.Int.Workshop on CdS Solar Cells and other Abrupt Heterojunctions, University of Delaware, New York, (1975)p.9.

136. W. Palz, J.Besson, J.N.Duy and J.Vedel, Proc. 10th IEEE Photovoltaic Specialists Conf. Palo Alto, C.A.(1973) p.69.

137. L.C.Burton: Solar Cells 1 (1979/80), p.159.

138. E.A.Davis and E.L.Lind: J.Phys.Chem.Solids, 29 (1968), p.79.

139. D.W.G. Ballentyne and B.Ray: Physica 27 (1961) p.337.

140. L.C.Burton, T.L.Hench and J.D.Meakin: J.Appll.Phys. 50 (1979) p.6014.

141. L.C.Burton and T.L.Hench, Appl.Phys.Lett. 29 (1976), p.612.

142. R.S.Feigelson, A.N. Diaye, S.Y.Yin and R.H.Bube, J.Appl.Phys. 48 (1977) p.3162.

143. V.P.Singh and J.F.Jordan: IEEE Electron Device.Lett. (USA) Vol.EDL-2, No.6 (1981) p.137.

CHAPTER 3

THEORY OF THE CdS/Cu_2S JUNCTION

3.1 INTRODUCTION

In this Chapter some of the basic theory required for understanding the CdS/Cu_2S junction is briefly described. The current voltage characteristic and various parameters affecting the junction performance are described in a qualitative way. Mathematical expressions are developed wherever necessary. The effect of interfacial recombination which is an important process in the junction is discussed in detail. The Chapter closes with a description of capacitance-voltage characteristics and the photocapacitance techniques which are used to identify and characterize the defect levels in the space charge region of Schottky diodes and the CdS/Cu_2S heterojunction.

3.2 THEORY : GENERAL ASPECTS

The solar cell can be represented electrically as a light dependent current generator in parallel with a diode. Additional resistance arises from the bulk n- and p-layers and the contacts, giving rise to a series resistance, R_s. Losses occur from the junction leakage and alternative current paths providing a parallel or shunt resistance across the diode. The resulting equivalent circuit is presented in Figure 3.1.

In general the current through solar cell can be described by the following equation which is a super-position of the dark and light generated current[1].

$$J - \frac{V-JR_s}{R_{sh}} = \sum_i J_{oi} \left\{ \exp\left[\frac{q}{A_i kT}(V-R_s J)\right] - 1 \right\} - J_L(v) \qquad (3.1)$$

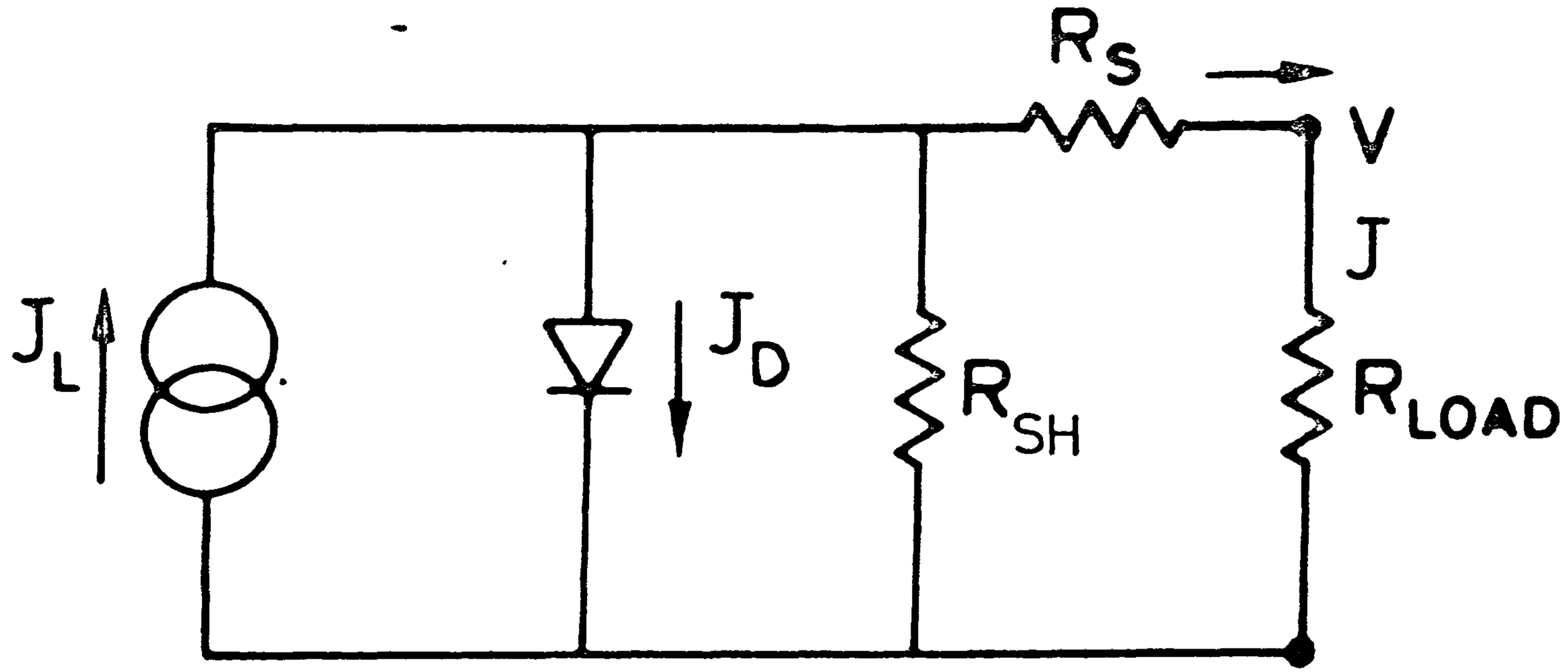


FIGURE 3.1: Simplified equivalent circuit for solar cells

J_L is the light generated current and may be voltage dependent. If series and shunt resistance effects are negligible, J_L is equal to the short circuit current which is the current that flows through the junction under illumination at zero applied bias. A_i is the diode factor. It usually varies between 1 and 2. J_{oi} represents the reverse saturation current. The sum over i indicates various contributions to the diode current which can occur. These include (1) the ideal diffusion or emission currents (2) recombination generation currents which are characteristic of the depletion or space charge region on either side of the junction (3) recombination through interface states at the junction (4) tunnelling from band states to localized defect states in the gap, across the interface (5) band to band tunnelling.

For a homojunction $A_i = 1$ and when the current mechanism is ideal diffusion, the reverse saturation current is given by

$$J_o = q \left[\frac{D_n}{L_n} n_{op} + \frac{D_p}{L_p} p_{on} \right] \qquad (3.2)$$

where q is the magnitude of the electronic charge, D_n the electron diffusion coefficient, and L_n the diffusion length of electrons in p-type material. D_p and L_p are the corresponding quantities in the n-type material and n_{op} and p_{on} are the equilibrium densities of electrons and holes in p- and n-type material. The diffusion coefficients and lengths are related to basic material properties via the equations $D = kT\mu/q$, $L = (D\tau)^{1/2}$, where μ is the mobility and τ the recombination lifetime of the minority carriers. Sometimes recombination takes place in the space charge region and in that case $A_i \simeq 2$ and $J_o \sim \exp(-Eg/2kT)$[1].

For Schottky diodes, if the space charge region is small, the reverse saturation current is given by

$$J_o = A^* T^2 \exp\left(\frac{q\phi_B}{A_i kT}\right) \qquad (3.3)$$

where $A^* = 120 \left\{ \frac{m^*}{m_o} \right\}$ amp/cm^2.K^2 is the modified Richardson constant for thermionic emission. m^* is the effective mass and ϕ_B is the barrier height. If the space charge region is wide the diffusion currents of charge carriers modify the equation to

$$J_o = \frac{q\, N_C\, v_R}{1 + v_R/v_D} \exp\left(-\frac{q\phi_B}{kT}\right) \tag{3.4}$$

Here N_C is the effective density of states, $v_R = \frac{AT^2}{qN_C}$ and v_D is an effective diffusion velocity.

For an MIS solar cell, the saturation current density is similar to that for a Schottky barrier with an additional tunnelling term[2] and can be written as

$$J_o = A^* T^2 \exp\left(\frac{-q\phi_B}{kT}\right) \exp\left[-(q\phi_T)^{\frac{1}{2}} \delta\right] \tag{3.5}$$

where $q\phi_T$ is the average barrier height presented by the insulating layer and δ is the insulator thickness.

In heterojunctions the carrier transport properties are dominated by processes in the interface region such as recombination, and tunnelling or tunnelling and recombination involving energy levels near the interface. The theoretical treatment becomes more complicated with the presence of discontinuities in the conduction and valence bands associated with the difference in the bandgaps (Eg) and electron affinities (χ) of the semiconductors. (The electron affinity is defined as that energy required to raise an electron from the conduction band to the vacuum level, which in a metal corresponds to the work function). When two semiconductors are brought together the alignment of the Fermi level and the continuity of the electric displacement at the interface leads to these discontinuities.

Several different transport models have been proposed for the heterojunction and they are discussed in detail in Refs (3) and (4). The basic

model is an extension of Schottky diode theory to a heterojunction with no interface states (the Anderson model)[5,6]. Transport is then diffusion dominant. This is an ideal situation. Experimentally, the observed J-V characteristics are different from those predicted by this model. The differences are attributed to the presence of defects at the junction. In general the J-V characteristic for a heterojunction can be represented by the equation [7].

$$J = J_{oo} \exp(-\Delta E/kT) \left[\exp\left(\frac{qV}{A\ kT}\right) - 1 \right] \qquad (3.6)$$

where J_{oo} and A may be slowly varying functions of T and V, and E is a measured activation energy from the zero bias extrapolation of Ln J versus V curves. In those cases where the relationship between log J and V is relatively temperature independent, the junction characteristic fits the relation

$$J = J_{oo}'' \exp(\beta T) \exp(-\alpha\phi_b) \exp(\alpha V) \qquad (3.7)$$

where β and α are fairly constant and relatively temperature independent.

Generally speaking, imperfection levels are introduced at the interface of a heterojunction as a result of lattice mismatch between the two semiconductors, and from impurities or defects introduced during fabrication. The difference in the lattice constants of the two semiconductors causes a breakdown in the periodicity in the crystalline structure and thus produces edge dislocations with associated dangling bonds[8]. These edge dislocations form a regular net at the interface and each dislocation core is surrounded by a region of lattice strain (see Figs 3.2a and b). The density of the resultant interface states has been estimated to be $N_1 \sim \frac{2\Delta a}{a^3}$ where Δa

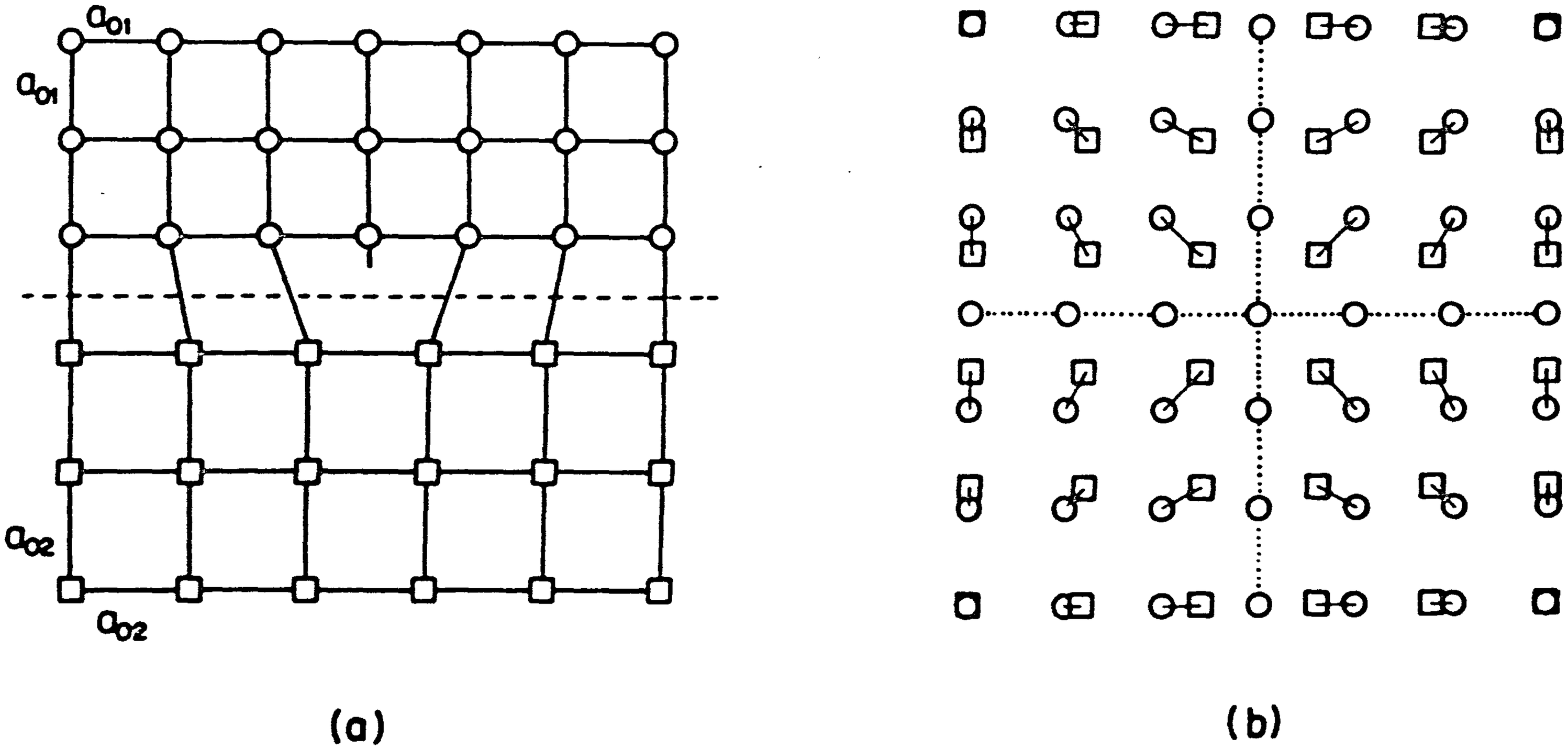


FIGURE 3.2: Schematic diagrams of the interface of two cubic single crystals with different lattice parameters (Ref 7).
(a) A view parallel to the interface plane showing the end view of a pure edge dislocation
(b) A view perpendicular to the interface plane showing a pair of orthogonal dislocations
(The circles and squares represent the interfacial layers of atoms on either side of the boundary of the two materials.

is the difference in lattice constant in the plane of the junction and a is the average lattice constant.

Not all the interface states need be electrically active. Many are compensated so that only a small fraction remains active to account for the observed electrical phenomena[9]. Interface states acting as charge traps are considered to be donors if they are electrically neutral when filled with electrons and positive when empty. They are acceptor like if they are neutral when empty and negative when filled with electrons. The situation where the negative charge is bound by an interstitial ion, (itself a positively chargeddonor) is assumed to create a permanent-interfacial dipole with its own potential energy contribution. Van Ruyen assumed that a large number of surface states on a semiconductor is equivalent to a metallic layer which pins the Fermi level[10]. Recently, Fonash[11] has discussed the properties of interface states in detail.

The presence of a large density of electrically active interface states distorts the band profile, raising or lowering the conduction bands at the interface with respect to the equilibrium Fermi level. The states also provide a large density of recombination centres which can explain the high observed values of J_o.

3.3 INTERFACIAL RECOMBINATION IN CdS/Cu_2S SOLAR CELLS

In the CdS/Cu_2S cell there is a 4% lattice mismatch between Cu_2S and CdS so that a large density (about 10^{13} cm^{-2}) of interface states exists at the junction. The three major mechanisms which contribute to the diode current J_o are as follows:-

(1) thermally excited electrons in the CdS diffuse into the quasi neutral region of the Cu_xS and recombine with holes,

(2) thermally excited electrons in the CdS flow through interface states to recombine with holes at the interface in Cu_xS,

(3) electrons in the CdS with or without thermal assistance, tunnel through into interface states with subsequent recombination with holes in the Cu_xS at the interface.

In CdS cells the second process of interface recombination dominates. The reverse saturation current is given by[12]

$$J_o = q\ N_C\ S_I \exp\left(\frac{-q\phi}{kT}\right) \qquad (3.8)$$

where S_I is the interfacial recombination velocity $S_I = v_{th}\ \sigma\ N_I$, N_I is the effective density of interface states, σ is the capture cross section of the interface states and v_{th} is the thermal velocity of electrons. For the CdS/Cu_2S solar cell, S_1 has been estimated to vary between $10^5 - 5 \times 10^6$ cm s^{-1} (12).

ϕ is the activation energy or barrier height to electron flow between the n and p sides of the junction and is described by the relation (see Fig 3.3)

$$\phi = Eg_1 - \delta_1 - q\ V_{DP} - \Delta\chi_1 \qquad (3.9)$$

where $\Delta\chi$ is the difference in the electron affinities of CdS and Cu_2S, δ_1 is the separation between the valence band and Fermi level in Cu_2S, V_{DP} is the diffusion voltage in Cu_2S which is related to the diffusion voltage in CdS by $V_{DP} = V_D \dfrac{N_D}{N_A + N_D}$, where N_D and N_A are the uncompensated donor and acceptor densities in CdS and Cu_2S. The position of the Fermi level is related to the carrier densities by the equation $\delta_1 = kT\ Ln\left\{\dfrac{N_V}{N_A}\right\}$ and $\delta_2 = kT\ Ln\left\{\dfrac{N_C}{N_D}\right\}$ where N_C and N_V are the intrinsic carrier densities.

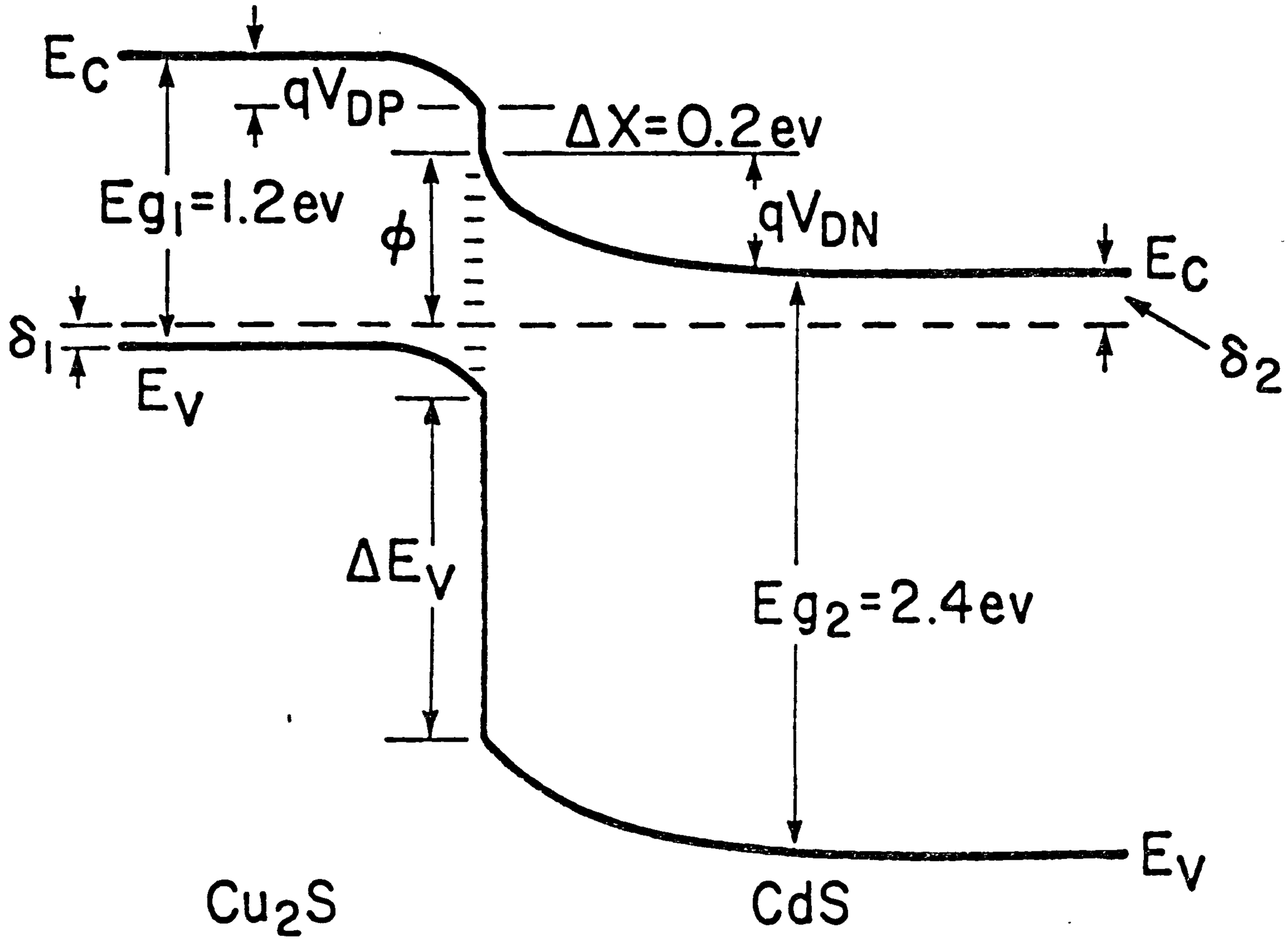


FIGURE 3.3: Energy band diagram of CdS/Cu_2S heterojunction (Ref 13)

3.4 LIGHT GENERATED CURRENT

On illumination the light generated current is produced primarily by the absorption of photons in the Cu_2S layer. However, the light reaching the CdS layer plays a very important part in 'gating' the flow of electrons through the interface region. In the steady state, J_{LO}, the injected electron density, J_{LR}, the current density lost at the interface through interface recombination, and J_L the current density which passes through the external circuit are determined by (see Fig 2.7).

$$J_{LO} = J_{LR} + J_L \tag{3.10}$$

At the junction $$J_{LR} = q\, n_1\, S_I \tag{3.11}$$

$$\text{and } J_L \simeq q\, n_1\, \mu_2\, F_2 \tag{3.12}$$

where n_1 is the density of electrons at the junction, μ_2 the mobility of electrons in CdS and F_2 the field at the interface. It follows that

$$J_L = J_{LO} \quad \frac{\mu_2\, F_2}{S_I + \mu_2\, F_2} \tag{3.13}$$

The term $\dfrac{\mu_2\, F_2}{S_1 + \mu_2\, F_2}$ is called the interfacial collection factor (ICF). ICF = 0.5 when $\mu_2\, F_2 = S_I$ and approaches unity asymptotically for large $\mu_2 F_2$.

The junction field F_2 is given by the following equations[13]:

Under zero bias

$$F_2\,(0) = \frac{2\, V_D}{w} = \frac{2\, V_D\, C}{\epsilon_o \epsilon_s\, A} = \left(\frac{2\, V_D\, q\, N_D}{\epsilon_o \epsilon_s} \right)^{1/2} \tag{3.14}$$

In short circuit conditions

$$F_2(V) = \left\{ \frac{2q\, N_d\, (V_D - V)}{\epsilon_o \epsilon_s} \right\}^{1/2} \qquad (3.15)$$

where V_D is the diffusion voltage, w the width of space charge region, ϵ_s the dielectric constant of CdS (~ 3.64), ϵ_o the permittivity of free space (8.85×10^{-14} F/cm) and C the total capacitance of the junction. Thus the field is directly related to the total positive charge in the CdS space charge region and depends on the bias voltage.

Normally native defects or foreign dopants in CdS lead to the formation of shallow and deep levels. In the fabrication of a CdS/Cu_2S junction, a post barrier heat treatment is usually administered. Copper diffuses into CdS and forms deep acceptor levels in the depletion region[14-17]. This process compensates the donors, and the depletion width widens. Under illumination, holes are captured in these deep copper centres. The depletion width shrinks and the capacitance of the junction increases. Under AM 1 illumination the field has been found to be from 1-2 x 10^5 V cm^{-1}, one order higher than its value in the dark. The corresponding value of ICF was about 0.95[13]. The overall effect of all these parameters can be seen by substituting the values of J_o and J_L in Eq. 3.1. Neglecting the term $\frac{J R_s}{R_{sh}}$, which is very small, the current-voltage equation for a CdS/Cu_2S cell can be written

$$J = \frac{V}{R_{sh}} + q N_C S_1 \exp\left\{ - \frac{q\phi}{kT} \right\} \left\{ \exp\left[\frac{q}{A_i kT} (V - R_s J) \right] - 1 \right\} - \frac{\mu_2 F_2}{S_I + \mu_2 F_2} J_{LO} \qquad (3.16)$$

3.5 CELL EFFICIENCY

Typical current voltage characteristics for a CdS/Cu_2S cell in the dark and under illumination are shown in Fig (3.4). The maximum power is determined from the J-V curve by finding the rectangle of the largest area under the J-V curve in the fourth quadrant. The product of the voltage at the maximum power point (V_{mp}) and current (J_{mp}), gives the maximum power output. It is customary to describe the maximum power output as a fraction of the product of the open circuit voltage and short circuit current. This fraction is called the Fill factor, FF

$$FF = \frac{J_{mp} \times V_{mp}}{J_{sc} \times V_{oc}} \qquad (3.17)$$

The efficiency which is the ratio of the maximum power obtained from the cell to the incident power is then expressed as

$$\eta = \frac{P_{max}}{P_{in}} = \frac{J_{sc} \times V_{oc}}{P_{in}} \times FF \qquad (3.18)$$

Higher values of SCC, OCV and FF are therefore desirable if efficient solar cells are to be obtained.

3.5.1 Solar Radiation

The incident photon flux density depends upon the available solar radiation. The intensity of solar radiation in free space at the average distance of the earth from the sun is defined as the solar constant, which has a value of 1353 W/m^2. The atmosphere attenuates the sunlight reaching the earth's surface, mainly by absorption by water vapour in the infrared, ozone absorption in the ultra violet, and scattering by airborne dust and aerosols. The degree to which the atmosphere affects the sunlight received at the earth's surface is defined by the 'air mass'. The secant of the angle between the sun and the zenith (sec θ) is called the 'air mass' and

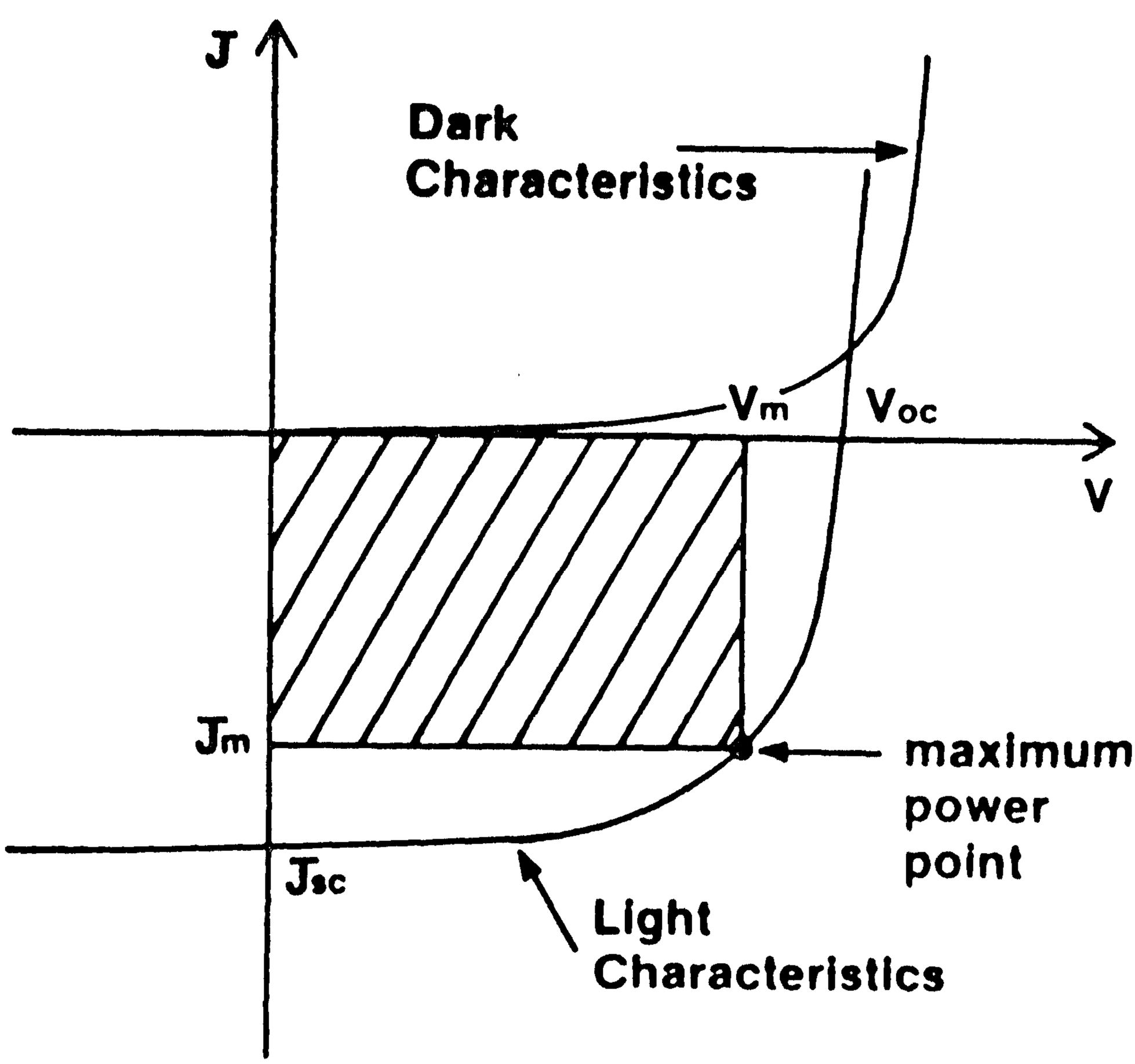


FIGURE 3.4: Typical dark and light J-V characteristics of a CdS/Cu_2S solar cell

measures the atmosphere path length relative to the minimum path length when the sun is directly overhead.

In Fig (3.5) the upper curve represents the solar spectrum outside the earth's atmosphere. This is the air mass zero (AMO) condition. The AMO spectrum is the relevant one for satellite and space vehicle applications. The AM1 spectrum represents the sunlight at the earth's surface when the sun is at zenith ; the incident power is about 1000 W/m^2. The AM2 spectrum is for $\theta = 60^o$ and has an incident power of about 690 W/m^2. Concentrators are sometimes used to increase the photon flux, but diurnal tracking is necessary to follow the sun and this makes the system more complicated.

3.5.2 The Short Circuit Current

It is obvious that to obtain larger values of SCC the ICF should be larger, and J_{LO} should also have a higher value (Eq. 3.13). The ICF is determined by the field (F_2) and interfacial recombination velocity (S_I). Reducing the interface state density would contribute to the enhancement of the ICF. The other features have been discussed in Section 3.1.

J_{LO} is determined principally by the incident photon flux density, the reflection losses and the collection efficiency of the Cu_2S layer, which is a function of the absorption coefficient, diffusion length L, effective thickness, grain size, drift field and surface recombination velocity. The stoichiometry of Cu_xS therefore plays an important role.

Rothwarf and Barnett[18] estimated that the total losses in J_{sc} for the front wall cell include 15% from recombination in the bulk Cu_2S, 5% from the recombination at the interface between the Cu_xS and the CdS, 4% from grid shadowing, 5% from light absorption and reflection losses in the encapsulating layer, and 1% each for recombination losses at the front surface and at grain boundaries. In a poorly optimized device cell the interfacial recombination losses can be as high as 30-40% of the current. In an ideal situation, without any loss, the maximum SCC from a CdS solar cell can be 35 mA/cm^2.

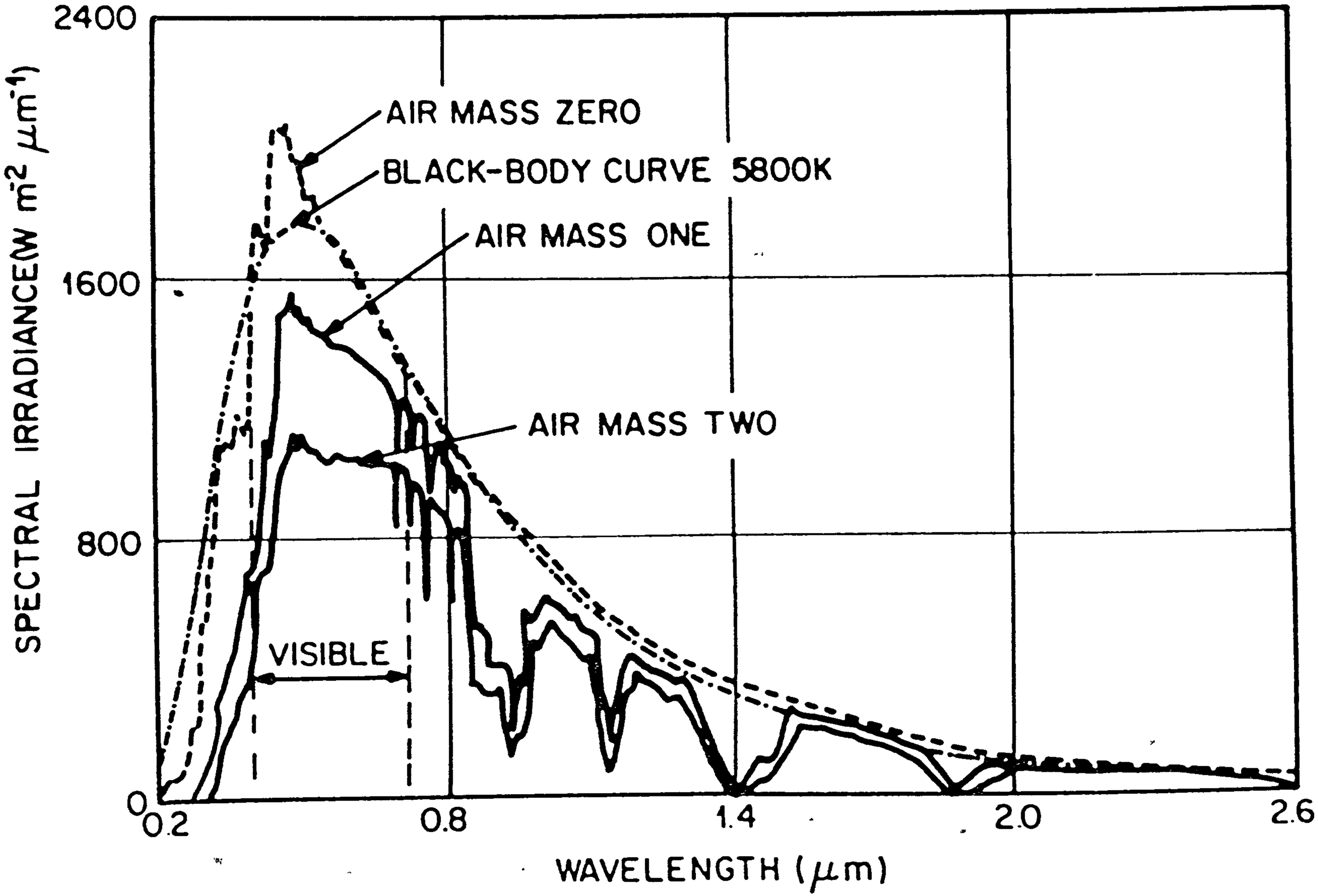


FIGURE 3.5: Spectral distribution of solar radiation under different conditions

3.5.3 Open Circuit Voltage

The open circuit voltage can be expressed in the following way provided the shunt resistance is very high

$$q\,V_{oc} = Eg - \Delta\chi + kT \quad Ln \left(\frac{J_L}{q\,N_C\,S_I} \right) \tag{3.19}$$

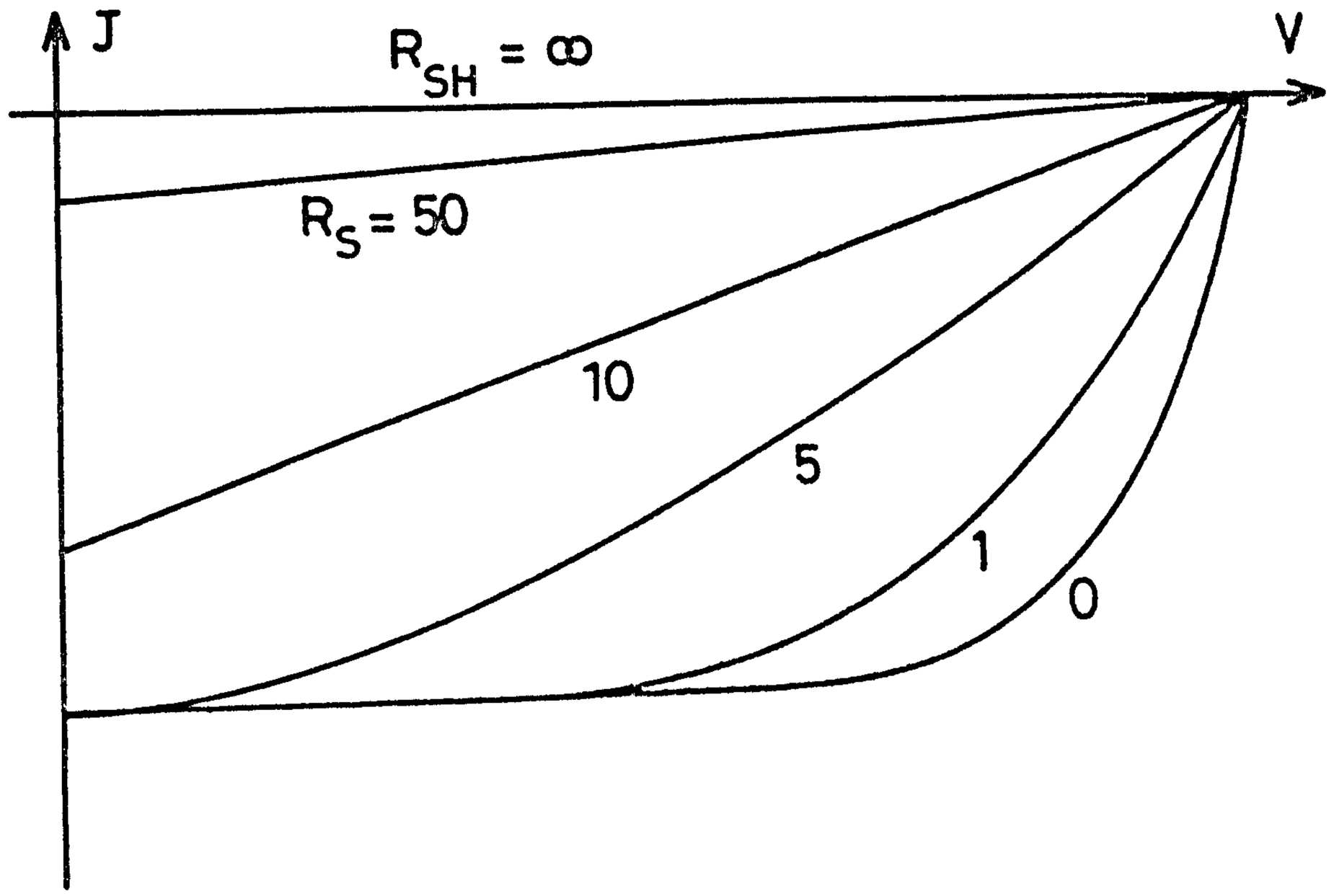
The fundamental dependence of V_{oc} on S_I is evident in this equation. As long as $\Delta\chi$ is large and S_I is reasonably large, the open circuit voltage will be less by an amount $\Delta\chi$, than it would be in a junction with matched electron affinities. Another factor that affects V_{oc} is the crystallite size. Rothwarf[19] reported a loss in OCV due to the effective junction area by as much as 0.06V as determined from the equation

$$\Delta V_{oc} = kT \quad Ln \quad \frac{A_1}{A_j} \tag{3.20}$$

where A_1 and A_j are the planar and actual junction areas. It is obvious that to increase the OCV, $\Delta\chi$ should be small and S_I should be a minimum. $Cd_{1-y}Zn_yS$ has therefore been used to reduce the difference in the electron affinities and lower the value of S_1. If $\Delta\chi = 0$ and $S_1 = 0$, the current mechanism would be diffusion dominated and it has been estimated by Burton[20] that an OCV as high as 0.85V should be obtained for such a $Cd_{1-y}Zn_yS/Cu_2S$ cell.

3.5.4 Fill Factor

The parameters that affect the fill factor are primarily the series and shunt resistances R_s and R_{sh}. The effect of these parameters on the J-V characteristics is shown in Fig (3.6). It is obvious that as the series resistance increases and shunt resistance decreases, the fill factor



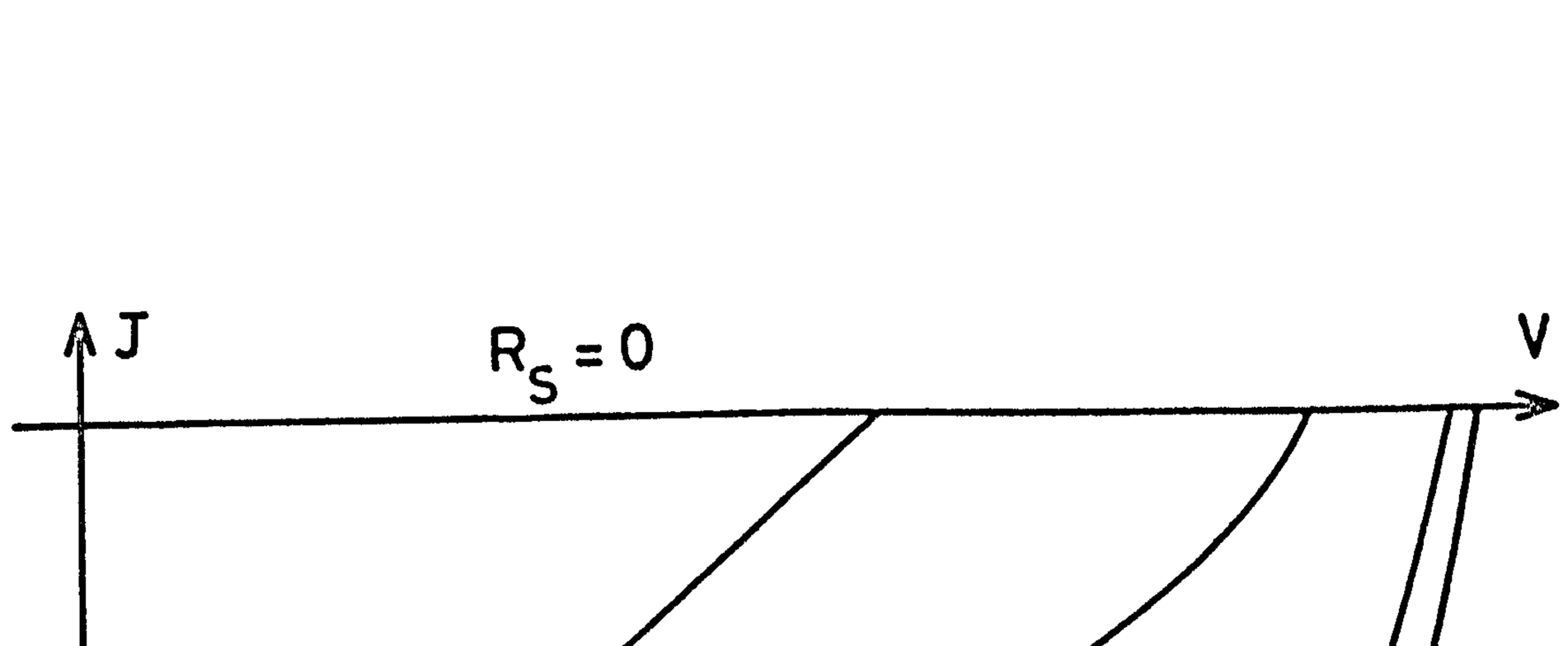


FIGURE 3.6: Effect of series and shunt resistance on J-V characteristics of a solar cell. (Ref.21)

deteriorates. To a first approximation R_s and R_{sh} can be evaluated using the equations[21]

$$R_s = \lim_{V \to V_{oc}} \left(\frac{dJ}{dV}\right)^{-1} \quad \text{and} \quad \frac{1}{R_{sh}} = \lim_{V \to 0} \left(\frac{dJ}{dV}\right) .$$

In CdS/Cu_2S cells since the field is voltage dependent, there is a further effect upon the fill factor. Rothwarf[13] summarizes all these contributions in the following equation

$$FF = FF_o \left(\frac{q\, V_{oc}}{kT}\right) - (\Delta FF)_{R_s} - (\Delta FF)_{R_{sh}} - (\Delta FF)_{F_2} \qquad (3.21)$$

where the first term is the theoretical loss factor which is a function of V_{oc}/kT. $(\Delta FF)_{R_s}$ is the loss in fill factor due to the series resistance

$$(\Delta FF)_{R_s} = C \left(\frac{q\, V_{oc}}{kT}\right) J_{sc} \cdot \frac{R_s\, A_1}{V_{oc}} \qquad (3.22)$$

C is a constant $\tilde{\sim}$ 0.9, A_1 is the area of the cell.

$(\Delta FF)_{R_{sh}}$ is the loss in fill factor due to the shunt resistance and is given by

$$(\Delta FF)_{R_{sh}} = \frac{V_{mp}}{V_{oc} J_{sc} \cdot R_{sh} A_1} \qquad (3.23)$$

Finally $(\Delta FF)_{F_2}$ is the loss in fill factor due to the voltage dependence of field

$$(\Delta FF)_{F_2} = \frac{V_{mp}}{V_{oc}} S_I \frac{1 - F_2(V_{mp})/F_2(o)}{S_1 + \mu_2 F_2/V_{mp}} \qquad (3.24)$$

This loss can account for the charge in fill factor with different wavelengths of illumination[22].

In a heat treated CdS/Cu_2S junction, the shunt resistance is normally very high and its contribution towards the loss in fill factor is small compared with that of the series resistance. The major contribution to R_s is the resistance of the Cu_xS layer and the electrical contacts if the CdS layer is highly conducting. For an optimized grid, the series resistance has been evaluated[12] as $R_s A_1 = \frac{\rho_1 s^2}{12\, d_1}$ where ρ_1 is the resistivity of the Cu_2S layer, d_1 its thickness and s the spacing between parallel grid lines.

3.6 MEASUREMENT OF SERIES RESISTANCE

Several suggestions have been made to deal with the effect of series resistance in a solar cell. Wolf and Rauschenbach[23] developed a self-consistent procedure to measure the series resistance, while Handy[24] has given a theoretical treatment. With his suggested method the series resistance can be evaluated by measuring the J-V characteristic under several different intensities of illumination. The method is time consuming and difficult. Chaffin and Osbourn[25] proposed a simplified scheme which employed a single pulsed illumination technique. The method is based on the logarithmic dependence of SCC at very high intensities. The current voltage characteristic in the presence of a load R_L is given by,

$$J = J_o \exp\left[\left(\frac{q\, V_d}{A\, kT}\right) - 1\right] - J_L \qquad (3.25)$$

Under illumination the voltage drop across R_L and R_S is V_d and if $J >> J_o$, the equation can be re-written as[25]

$$J = J_o \left(\exp \frac{q\, J(R_L + R_S)}{A\, kT}\right) - J_L \qquad (3.26)$$

For very high intensities

$$J_o \exp \left\{ \frac{q\ J\ (R_L + R_S)}{A\ kT} \right\} >> J$$

The equation (3.25) reduces to

$$J_L \simeq J_o \exp \left[\left(\frac{q\ J}{A\ kT} \right) \quad (R_S + R_L) \right]$$

$$\text{or} \qquad J \simeq \frac{AkT/q}{R_S + R_\ell} \quad \text{Ln} \quad \left(\frac{J_L}{J_o} \right) \tag{3.27}$$

If J increases logarithmically with light intensity the equation can be used to determine the internal series resistance. This is done by making measurements at the maximum available light intensity using two different known values of R_L. Since J_L will be constant, it can be shown that

$$R_S = \frac{J_2 R_{\ell_2} - J_1 R_{\ell_1}}{J_1 - J_2} \tag{3.28}$$

The subscripts 1 and 2 refer to measurements with load resistors 1 and 2. This technique was originally applied to the GaAlAs cell. It has been used in this work with the CdS-Cu_xS cell.

3.7 CAPACITANCE - VOLTAGE CHARACTERISTICS

3.7.1 Schottky Barriers

The capacitance of the sample is determined by the distribution of the charge density ρ in the space charge region of the junction. With a Schottky barrier device which is the simplest junction, and assuming that the charge density ρ in the depletion region is given by $\rho = q\ N_d$ ($N_d = N_D - N_A$ = donor density) for $x < w$ and $\rho = 0$ for $x > w$ (w = depletion

width), integration of Poisson's equation yields[2]

$$V(x) = \frac{q N_d}{\varepsilon_o \varepsilon_s} \left(w x - \frac{1}{2} x^2\right) - \phi \qquad (3.29)$$

The electric field then becomes

$$|E(x)| = \frac{q N_d}{\varepsilon_o \varepsilon_s} (w-x) \qquad (3.30)$$

and the depletion width is

$$w = \left[\frac{2 \varepsilon_o \varepsilon_s}{q N_D} \left(V_d + V - \frac{kT}{q}\right) \right]^{1/2} \qquad (3.31)$$

where ε_s is the relative permittivity of the semiconductor, V_d is the diffusion potential at zero bias and $\frac{kT}{q}$ is a contribution from the kinetic energy of the mobile charge carrier. The space charge Q_{sc} per unit area and capacitance per unit area are given by

$$Q_{sc} = q N_d w = \left[2 q \varepsilon_o \varepsilon_s N_d \left(V_d + V - \frac{kT}{q}\right) \right]^{1/2} \qquad (3.32)$$

and

$$C = \frac{\partial Q_{sc}}{\partial V} = \frac{q \varepsilon_o \varepsilon_s N_d}{2 (V_d + V - kT/q)}^{1/2} = \frac{\varepsilon_o \varepsilon_s}{w} \qquad (3.33)$$

Thus the depletion layer capacitance is voltage dependent, and inversely proportional to the depletion width. The depletion width increases with reverse bias. w is inversely proportional to N_d, i.e. it narrows as the density of uncompensated donors increases. At higher temperature more donors are ionized and $N_d = N_D^+ - N_A^-$ is large, so that the depletion

region is smaller. At lower temperatures N_d decreases and w increases

Eq. (3.32) may be re-written as

$$\frac{1}{C^2} = \frac{2\ (V_d + V - \frac{kT}{q}\ )}{q\ \epsilon_o \epsilon_s\ N_d} \qquad (3.34)$$

or

$$N_d = \frac{2}{q\ \epsilon_o \epsilon_s} \quad \frac{d\ V}{d(C^{-2})} \qquad (3.35)$$

Providing that N_d remains constant throughout the depletion region, a plot of $\frac{1}{C^2}$ vs V should produce a straight line, the voltage intercept of which gives the diffusion potential V_d, while the gradient yields the donor density N_d. If there are electron traps present in the depletion layer then some traps above the Fermi level will be emptied when reverse bias is applied. This would contribute an additional capacitance. Depending on whether or not the trap concentration is large compared with the donor density, a plot of $1/_C2$ vs V will be either a straight line or have a downward concave curvature[26].

With thin films, the intergranular barriers also provide depleted regions in the grains at the interfaces and may affect the capacitance measurements. For details see Ref (11).

3.7.2 The CdS/Cu_2S Heterojunction

In the CdS/Cu_2S heterojunction the net acceptor density is about 10^{19} cm^{-3} or more in the Cu_2S, which is much larger than the net donor density in the CdS. Most of the depletion layer width (w) is in the CdS side of the junction therefore and Eq. (3.23) can then describe the capacitance voltage characteristic. A plot of $1/_C2$ against V should give a linear relationship. In fact linear plots are obtained with as-prepared

cells as expected, but after heat treatment the curves develop an upward convex shape[27]. Hall and Singh[28] developed a more comprehensive capacitance-voltage relationship for CdS/Cu_2S heterojunctions. They assumed that the space charge region consisted of a narrow (~ 100 Å) high density space charge layer at the interface, followed by an extended low density region leading finally to the bulk space charge. Fig(3.7) is a plot of ρ/q as a function of x for abrupt changes from one space charge region to the next. Solving Poisson's equation for this distribution of space charge with suitable boundary conditions leads to the following

$$\frac{1}{C^2} = \left(\frac{2}{A^2\ \varepsilon_o\varepsilon_s q\ (N_2 + N_3)}\right) V + \left(\frac{2}{A^2\ \varepsilon_o\varepsilon_s q\ (N_2 + N_3)}\right) X \left(V_D + \frac{q}{2\varepsilon_o\varepsilon_s}\ (N_3 d_2^{\,2} - N_1 d_1^{\,2})\right) \quad (3.36)$$

The depletion width is given by

$$W = \left(\frac{2\ \varepsilon_o\varepsilon_s(V_D + V)}{q(N_2 + N_3)} + \frac{N_3\ d_2^{\,2}}{(N_2 + N_3)} - \frac{N_1 d_1^{\,2}}{N_2 + N_3}\right)^{\frac{1}{2}} \quad (3.37)$$

In the as-prepared condition it can be assumed that $N_1 = N_3 = 0$ and then Eqs (3.35) and (3.36) reduce to

$$\frac{1}{C^2} = \frac{2}{A^2\ \varepsilon_o\ \varepsilon_s\ qN_2}\ (V_D + V) \quad (3.38)$$

$$W = \left(\frac{2\ \varepsilon_o\ \varepsilon_s(V_D + V)}{q\ N_2}\right)^{\frac{1}{2}} \quad (3.39)$$

Which is the conventional relation for a metal semiconductor Schottky barrier. After heat treatment, copper diffuses into the CdS

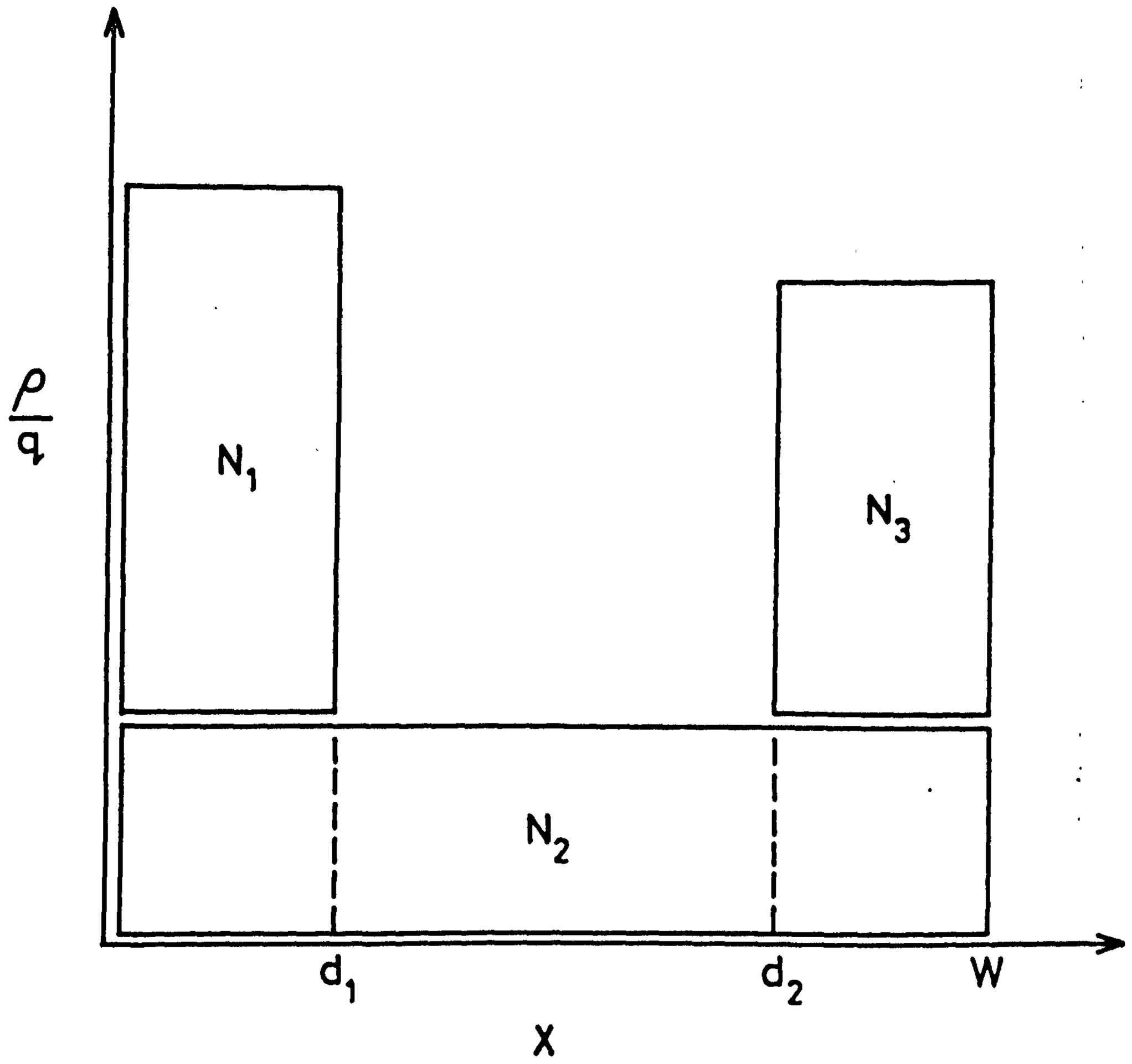


FIGURE 3.7: One dimensional spatial variation of space charge density (Ref 28)

and assuming that $N_1 > N_2$, $N_3 = 0$, we get

$$\frac{1}{C^2} = \left(\frac{2}{A^2 \varepsilon_o \varepsilon_s q N_2} \right) V + \frac{2}{A^2 \varepsilon_o \varepsilon_s q N_2} \left(V_D - \frac{q}{2\varepsilon_s} N_1 d_1^2 \right) \tag{3.40}$$

$$W = \left(\frac{2 \varepsilon_o \varepsilon_s (V_D + V)}{q N_2} - \frac{N_1}{N_2} d_1^2 \right)^{1/2} \tag{3.41}$$

If $d_1 < \left[2 \varepsilon_o \varepsilon_s (V_D + V)/q_1 N_1 \right]^{1/2}$, the slope of a plot of $1/C^2$ vs V still determines N_2 but the extrapolated intercept at the voltage axis is no longer the diffusion voltage V_D, but rather $V_D \; q/2\varepsilon_o \varepsilon_s \; N_1 d_1^2$.

If an insulating region is created by impurity compensation due to extensive heat treatment and $N_3 > N_2$; $N_1 = 0$, then

$$\frac{1}{C^2} = \frac{2}{A^2 \varepsilon_o \varepsilon_s q (N_2 + N_3)} V + \frac{2}{A^2 \varepsilon_o \varepsilon_s q (N_2 + N_3)} \left(V_D + \frac{q N_3 d_2^2}{2 \varepsilon_o \varepsilon_s} \right) \tag{3.42}$$

$$W = \frac{2 \varepsilon_o \varepsilon_s (V_D + V)}{q(N_2 + N_3)} + \left(\frac{N_3 d_2^2}{N_2 + N_3} \right)^{1/2} \tag{3.43}$$

The slope of the $1/C^2$ vs V plot is inversely proportional to $N_2 + N_3$. In all the cases traps in CdS would modify the characteristics[13].

The effect of an interfacial insulating layer on the capacitance has been analysed in some detail by Cowley [29] and Crowell and Roberts[30]. Recently Fonash[31] has presented a completely new model which describes all the possibilities for different types of interface states.

3.8 DEEP LEVELS

The stored charge in the deep energy levels is very significant in describing the junction capacitance. These levels affect the minority carrier lifetime significantly and are therefore very important in solar cells. An impurity in a semiconductor may act either as a trap or as a recombination centre, although a shallow impurity will often only act as a trap. If the captured carrier has a greater probability of being thermally re-excited to the free state, than of recombining with a carrier of opposite sign at the imperfection, the centre is a trapping centre or trap. On the other hand, if the capture carrier has a greater probability of recombining, the imperfection is a recombination centre. The capture of carriers is normally defined in terms of a capture cross section which reflects the ability to capture a free carrier. The mechanism includes the possibility of the capture into an excited state followed by relaxation to the ground state by exchange of phonons.

In considering capture processes of any centre, the sign of the charge carrier relative to the charge state of the centres is important, since this determines whether the process is attractive, neutral or repulsive. It is convenient to consider trapping centres with positive, neutral or negative charges (N_T^+, N_T^0 or N_T^-) when empty. For electron capture by an N_T^+ trap, the process is $N_T^+ + q \rightarrow N_T^0$ and the action is attractive. The generation process for the same trap is $N_T^0 \rightarrow N_T^+ + q$ and again is attractive. On the other hand, for a trap with an intrinsic negative charge N_T^- when empty, the capture process $N_T^- + q \rightarrow N_T^{2-}$, and is repulsive because of the Coulombic barrier around the charged trap. Therefore the capture cross section might be expected to be very small.

The values of the capture cross sections of a centre for both types of carriers reveal its electron or hole trapping nature. For recombination centres generally the capture cross section for both electron and holes are usually comparable.

The opposite process of capture is ionization, and this may be defined in terms of the probability of a centre emitting an electron or hole. Ionization may be achieved by thermal or optical processes. The optical ionization process is called photoionization and occurs at a rate, e_n^o, given by

$$e_n^o = \sigma_n^o \phi \tag{3.44}$$

σ_n^o is the photoionization cross section for electrons and ϕ is the photon flux.

The corresponding expression for holes is

$$e_p^o = \sigma_p^o \phi \tag{3.45}$$

3.9 PHOTOCAPACITANCE

Different space charge spectroscopic techniques have been used to identify and characterise deep energy levels[32,33,34]. Most of these make use of extrinsic excitation processes in the space charge region of a p-n junction or Schottky barrier. The change in the charge state and subsequent effect of this change on the capacitance of the depletion region brought about by exposure to light is called the photocapacitance. The sign of the change in capacitance (+ve or -ve), its magnitude and time dependence reveal the nature of the shallow and deep traps. Photocapacitance techniques have been used to identify defect levels in CdTe[35], GaP[36], ZnSe[37,38,39], CdS[40], and many other materials. The fundamentals of the methods are described by Grimmeiss and Ovren[41] and their application to II-VI compounds is summarised in Ref.(42).

The most convenient and simple method of identifying the defects in the space charge region is by measuring the steady state photocapacitance

spectrum by scanning the wavelength of the incident illumination. The threshold and the sign of the capacitance change identify the process of emptying or filling of the impurity level. Since the time constants for deep levels are long, a very slow scan speed is employed and sufficient time allowed for the steady state to be achieved. Although the overall picture of states in the depletion region can be obtained in this way, the actual capture cross sections can not be evaluated. This can be done by measuring the transient photocapacitance.

Since our interest is in the CdS/Cu_xS junction we consider a copper doped CdS sample where a deep acceptor state is formed with an excited hole state. The different processes which can occur, i.e. thermal and optical emission of electrons and holes are illustrated in Fig (3.8). For photon energies $h\nu < E_c - E_{Tg}$, the time dependence of the hole occupancy p_{Tg} of the ground state is given by

$$\frac{dp_{Tg}}{dt} = - e_p^{o} \; p_{Tg} \qquad (3.46)$$

where $e_p^{o} = \sigma_p^{o}\phi$ and σ_p^{o} is the photoionization cross section for the excitation of holes from the ground state into the valence band. Integrating Eq.(3.45) gives

$$p_{Tg}(t) = p_{Tg}(o) \exp(-t/\tau) \qquad (3.47)$$

where $\tau = \frac{1}{e_p^{o}}$ is the time constant.

If the holes are not excited directly into the valence band, but to the excited hole state first, from where they are thermally freed to the

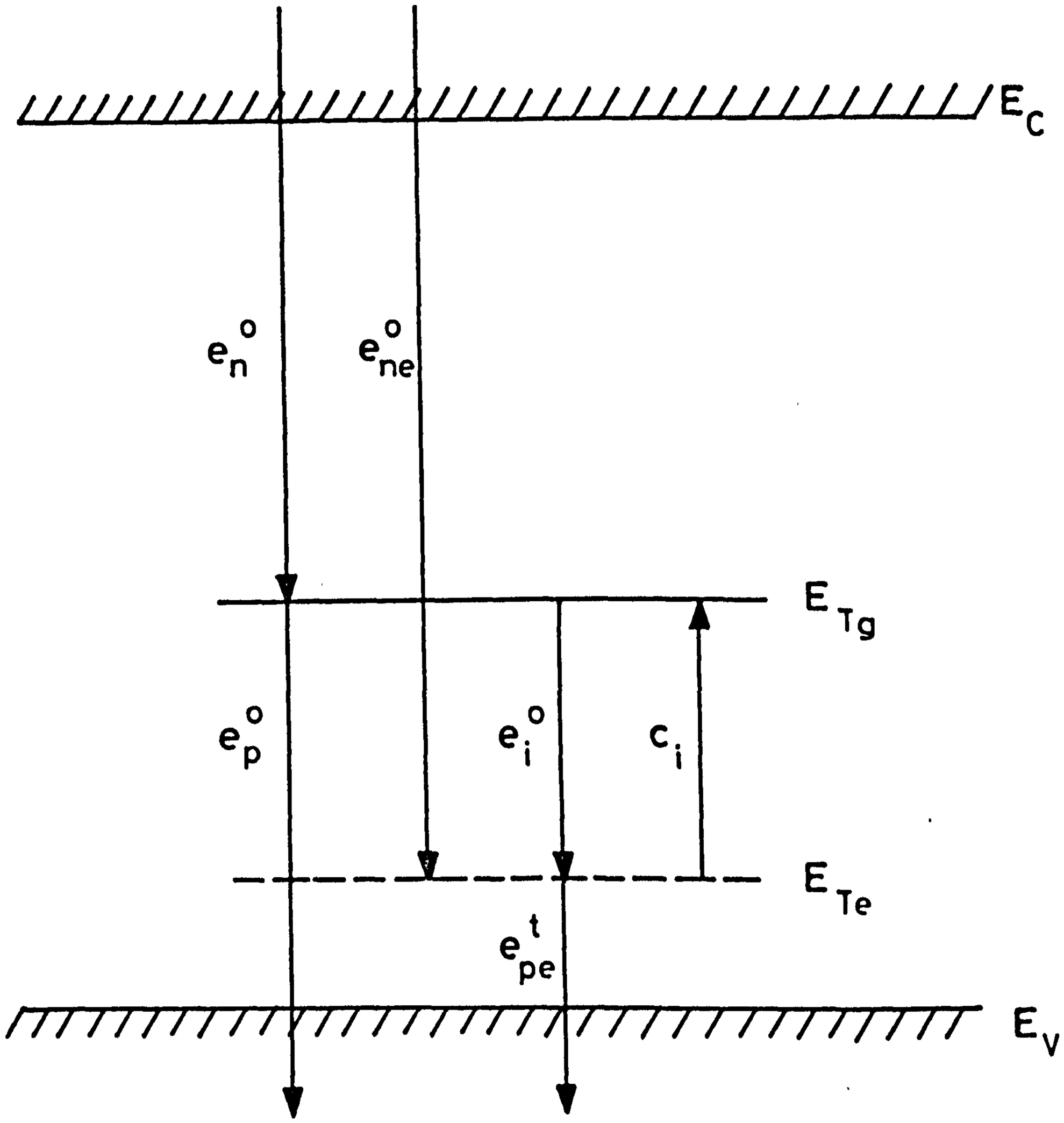


FIGURE 3.8: Energy level diagram for hole transitions in copper doped CdS.

valence band, Grimmeiss[40] has shown that

$$\frac{1}{\tau} = \left[e_{pe}^{t} \Big/ (e_{pe}^{t} + C_i) \right] e_i^{o} = C_2 e_i^{o} \qquad (3.48)$$

Here e_i^{o} is the optical excitation rate of holes from the ground state to the excited state, C_i is the de-excitation rate of holes from the excited state to the ground state and e_{pe}^{t} is the thermal emission rate of holes from excited state into valence band. The thermal processes freeze out if the temperature of measurement is reduced below 85K, then the time constant gives the emission rate of holes, and from a knowledge of photon flux the photoionization cross section for holes can be obtained.

Normally two methods are employed in the determination of capture cross sections using transient photocapacitance techniques. In the first method the photocapacitance is held constant by an applied bias voltage and transients of the bias voltage are recorded. These transients are directly proportional to the emission rate. The states are completely filled or emptied with an appropriate energy of light before starting the experiment. The other technique is known as infrared quenching of photocapacitance. Here the states are emptied by illuminating the sample with photon energy $h\nu_p \gtrsim Eg$. When a secondary illumination with $h\nu_s \simeq E_{Tg} - E_{Te}$ is used at higher temperature, or $h\nu_s \simeq E_{Tg}$ at lower temperature, electrons excited from the valence band are captured in the empty states and a quenching (reduction) in the photocapacitance is observed. The hole emission rate can be calculated from the time constant of the transient of infrared quenching[43]. Since copper diffuses in the CdS side of the CdS-Cu_2S cells, the technique enables us to identify the deep acceptor states in the depletion region of the heterojunction.

Infrared quenching of photocapacitance can also be used to measure the doping profile of the acceptors in the depletion region. If we distinguish $N_n(w)$ and $N_T(w)$ as the compensated donor density and acceptor impurity concentration (e.g. copper in CdS) then the following relation can be derived from Poisson's equation[43]

$$N_n(w_o)\ w_o dw_o = \left[N_n(w_s) - N_T(w_s) \right] w_s\ dw_s \qquad (3.49)$$

where o and s refer to irradiation with the primary light only and with the secondary light superposed respectively.

Then assuming $N_n(w_o) \simeq N_n(w_s)$ and

$$\frac{\Delta C_o}{C_o} = - \frac{\Delta w_o}{w_o} \quad \text{and} \quad \frac{\Delta C_s}{C_s} = - \frac{\Delta w_s}{w_s}$$

and using Eq.(3.35) for $N_n(w)$, the impurity concentration $N_T(w)$ can be calculated.

REFERENCES TO CHAPTER 3

1. A. M. Barnett and A. Rothwarf, IEEE Trans.Electron Devices ED-27 No.4 (1980), p.615.

2. S.M. Sze, Physics of Semiconductor Devices (Wiley, 1981).

3. A.L.Milnes and D.L.Feucht: Heterojunctions and Metal Semiconductor Junctions (Academic Press, New York,London, 1972).

4. B.L. Sharma and R.K.Purohit, "Semiconductor Heterojunctions (Pergamon Press, 1974).

5. R.L.Anderson: IBM J.Res.Dev 4 (1960), p.283.

6. R.L.Anderson: Solid State Electron. 5, (1962) p.341.

7. A.L.Fahrenbruch and R.H.Bube, "Fundamentals of Solar Cells - Photovoltaic Solar Energy Conversion" (Academic Press, New York, 1983).

8. W.G.Oldham and A.G.Milnes, Solid State Electron.7 (1964) p.153.

9. H.F.Matare : Defect Electronics in Semiconductor (Wiley,New York,1971).

10. L.J.Van Ruyen: Phys.Status Solidi 3 (1964) K 109-11.

11. S.J.Fonash, Solar Cell Device Physics (Academic Press, New York,1981).

12. A. Rothwarf, Proc.Int.Workshop on CdS Cells and other Abrupt Heterojunctions (Univ.of Delaware,Newark, May 1975) Tech.Rep. NSF-RANN AGR 75-15858) p.9.

13. A. Rothwarf, Solar Cells 2 (1980), p.115.

14. W.D.Gill and R.H.Bube: J.Appl.Phys. 41 (1970) p.3731.

15. W.G.Haines and R.H.Bube, IEEE Trans. on Elec. Devices ED27 (1980), p.2133.

16. T.Suda and S.Kurita ,J.Appl.Phys. 50 (1979) p.483

17. P. De Visschere, H.Pauwels L. Vandendriessche M.Burgelman and A. De Vos, Proc.5th EC P.S.E.C.Greece, (1983) p.878.

18. A.Rothwarf and A.M.Barnett: IEEE Trans.Electron Devices ED-24(1977) p.381.

19. A. Rothwarf, Conf.Rec.12th IEEE Photovoltaic Specialists Conf. (Baton Rouge, LA), Nov 1976, p.488.

20. L.C.Burton, Solar Cells. 1(1979/80) p.159.

21. R.Hill,'Thin Film Solar Cell in Active and Passive Thin Film Devices', ed. T.J.Coutts (Academic Press, 1978) p 487.

22. A. Rothwarf, J.Phillips and N.C.Wyeth, Proc.13th Photovoltaic Specialists Conf.Washington D.C,(1978) IEEE New York,1978, p.399.

23. M. Wolf and H.Rauschenbach, Adv.Energy Conv.3 (1963) p.455.

24. R.J. Handy : Solid State Electron.10 (1967) p.765.

25. R.J.Chaffin and C.C.Osbourn , Appl.Phys.Lett. 37 (1980), p.637.

26. A.M.Goodman, J.Appl.Phys. 34 (1963), 329.

27. A.L.Fahrenbruch and R.H.Bube, J.Appl.Phys. 45 (1974) p.1264.

28. R.B.Hall and V.P.Singh, J.Appl.Phys. 50 (1979), p.6406.

29. A.M.Cowley, J.Appl.Phys. 37 (1966) p.3024.

30. C.R.Crowell and G.I.Roberts, J.Appl.Phys. 40, (1969) p.3726.

31. S.J. Fonash, J.Appl.Phys.54 (1983) p.1966.

32. C.T.Sah, L.Forbes, L.L.Rosier and A.F.Tasch Jr. Solid State Electronics 13 (1970), p.759.

33. G.L. Miller, D. V.Lang and L.C.Kimerling, Ann.Rev. Mater.Sci.7 (1977) p.377.

34. H.G. Grimmeiss, Ann.Rev.Mat.Sci. (1977) p.341.

35. Y.Marfaing, J.Lascaray and R.Triboulet, Metal Semiconductor Contacts, Int.Phys.Conf.Ser.No.22 (1974), p.201.

36. H.G.Grimmeiss and G.O.Olofson, J.Appl.Phys. 40 (1969) p.2526.

37. F. Kosai, B.J.Fitzpatrick, H.G.Grimmeiss, R.N.Bhargava and G.F.Neumark, Appl.Phys.Lett. 35 (1979) p.194.

38. A.A.Qidwai and J.Woods, J.Crystal Growth, 59 (1982) p.217.

39. A.A.Qidwai and J.Woods, J. Phys. C.Solid St.Phys.,16 (1983) p.6789.

40. H.G. Grimmeiss, N. Kullendroff and R.Broser, J.Appl.Phys. 52 (1981), p.3405.

41. H.G.Grimmeiss and C. Ovren, J.Phys. E.Sci.Instrum. 14 (1981) p.1032.

42. H.G.Grimmeiss, J.Crystal Growth, 59 (1982) p.40.

43. T. Suda and R.H.Bube, J.Appl.Phys. 52 (1981) p.6218.

CHAPTER 4

EXPERIMENTAL TECHNIQUE

4.1 INTRODUCTION

In this chapter the more important experimental techniques and the equipment used in the present work are described. The chapter includes a brief account of crystal growth, the fabrication of hetero-junctions and the equipment required for the measurement of current voltage characteristics, spectral response, photocapacitance and series resistance. A few basic fundamentals of scanning electron microscopy and Reflection High Energy Electron Diffraction are also included.

4.2 CRYSTAL GROWTH

Some of the important features of the growth of CdS crystals have been discussed in Chapter 2 (see section 2.3.1). All the crystals were grown by the technique which was developed by Clark and Woods[1,2] and which uses a sealed silica tube in a vertical growth system. The CdS starting material was prepared by passing a continuous stream of argon down a furnace and over-heated polycrystalline CdS obtained from BDH. This led to the formation of crystalline platelets of CdS for use as charge material in the growth of large single crystals. In a quite separate purification, ZnS powder (also obtained from BDH) was outgassed and sublimed in a continuously pumped tube. For the growth of large single crystals a weighed quantity of CdS platelets was loaded into the growth ampoule, and when (Cd Zn)S crystals were to be grown a weighed quantity of vacuum sublimed ZnS was added to the charge. The ampoule was then evacuated and sealed using an oxy-gas flame. The experimental arrangement used for crystal growth with this system is illustrated in Fig 4.1. The charge was held at 1150^{o}C in the growth ampoule, which was

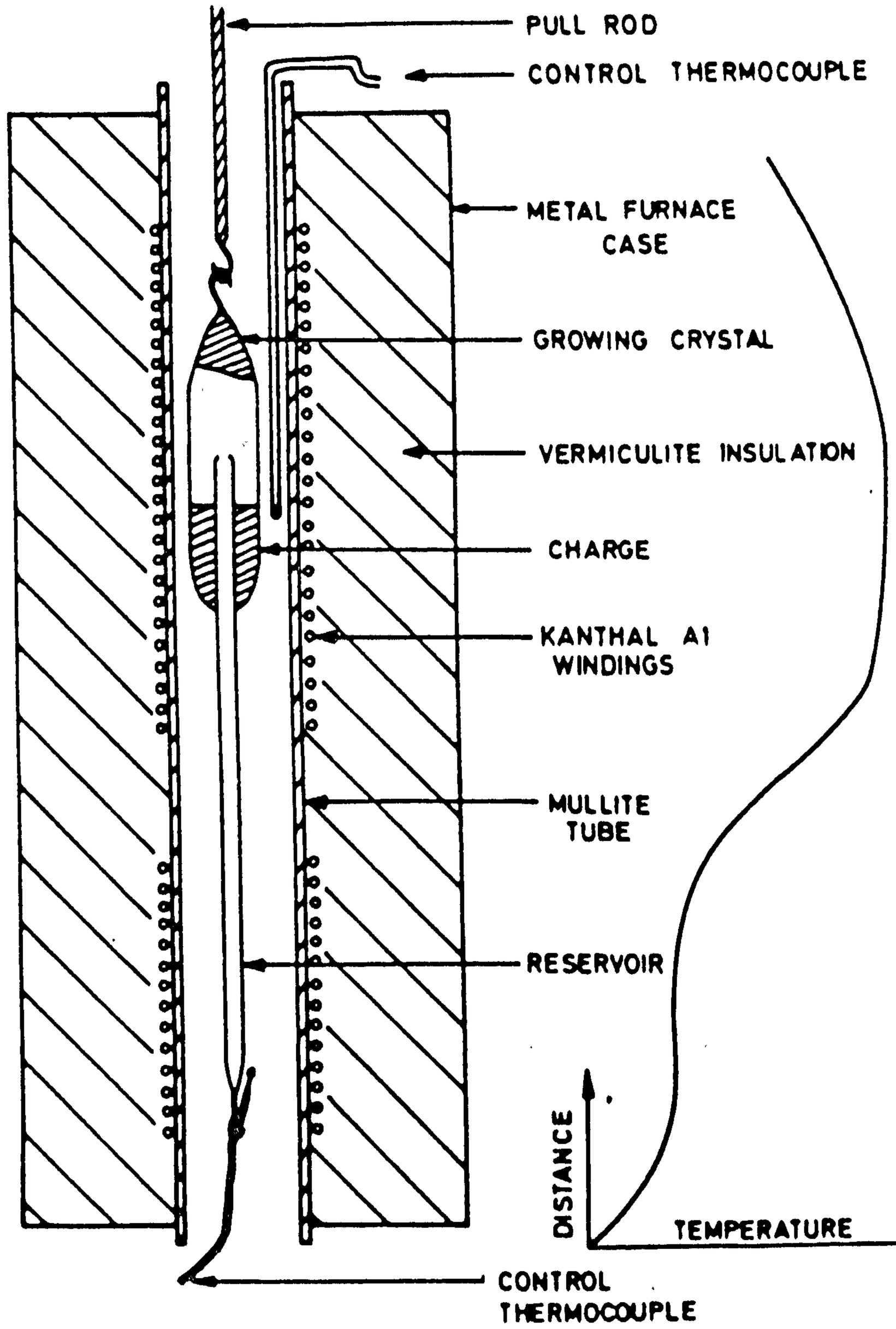


FIGURE 4.1: Experimental arrangements for the growth of CdS and (Cd Zn)S single crystals from the vapour phase.

connected via a narrow orifice to a long tail tube containing a reservoir of cadmium or sulphur. The temperature of the tail was adjusted to provide an appropriate vapour pressure of one of the elemental constituents over the evaporating charge. Higher reservoir temperatures were required as the zinc content of the mixed crystal increased. Generally with mixed crystals the charge was first converted to a solid solution of (Cd Zn)S in a reverse temperature gradient, then as the capsule was pulled and the growth gradient developed the various vapour species diffused to the cooler regions where supersaturation occurred and crystals grew.

Since the growth axis of a single crystal boule did not usually coincide with the c-axis, the technique of x-ray back reflection was used to orient the boules in order that they could be cut parallel to the basal $(00\bar{1})$ planes, to ensure that all devices might be fabricated on the same crystallographic surface. This eliminated any effects which might have arisen due to the use of planes of different orientation, especially considering the polar nature of the wurtzite structure.

4.3 HETEROJUNCTION FORMATION

Most of the heterojunctions were prepared by the dry barrier process, but a few devices were formed using the wet plating technique. The dry barrier process will be discussed in detail in Chapter 5. However, the arrangement of fittings in the 12" pump system bell jar used to evaporate CuCl is shown in Fig 4.2. Commercially available CuCl (which was green in colour due to the presence of $CuCl_2$) was first bleached with dilute HCl comprising 1 part HCl to 10 parts water. The powder was subsequently filtered, rinsed with acetone and finally dried in vacuum. The white CuCl which resulted was used in both processes of heterojunction formation.

The procedure for forming the Cu_xS layer by the wet plating technique can be summarised as follows[3,4].

(1) 75 ml of deionized water was heated in a closed reaction vessel while oxygen free nitrogen gas was bubbled through the liquid to remove any dissolved oxygen.

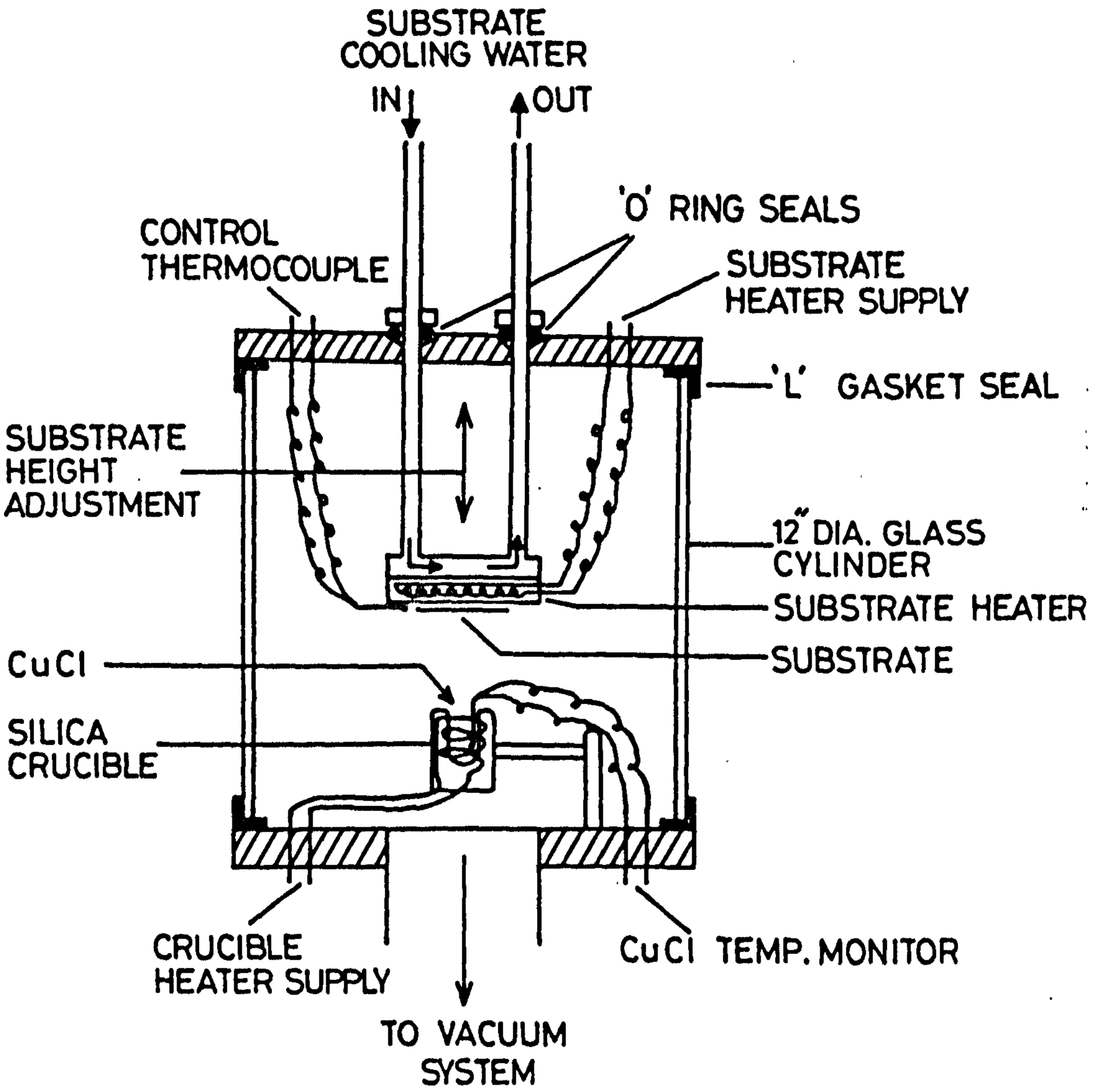


FIGURE 4.2: Evaporation system used for the deposition of CuCl.

(2) 12 ml of concentrated HCl acid was added to the water and heating continued while the nitrogen gas flow was maintained.

(3) 7 ml of hydrazine hydrate solution was added to the solution to produce a pH value between 2 to 3 as measured by narrow range pH papers.

(4) 1 gm of CuCl was added and the pH checked.

(5) After heating the solution to 95°C the pH was checked again and, if necessary, corrected by using a small amount of HCl or hydrazine hydrate.

(6) Chemiplating was carried out at about 95°C. To limit the growth of Cu_xS to the desired plane,all other faces of the crystal dice were masked with an acid resistant lacquer.

(7) The dice were pre-heated in deionized water at 95°C before plating.

(8) The dice were then immersed for 10 sec in the hot solution of CuCl, after which they were washed with deionized water and dried in a stream of nitrogen. The displacement reaction $CdS + 2\ CuCl \rightarrow Cu_2S + CdCl_2$ forms a topotaxial layer of Cu_2S on the surface of the CdS and the $CdCl_2$ goes into the solution.

4.4 REFLECTION HIGH ENERGY ELECTRON DIFFRACTION (RHEED)

RHEED studies were carried out in a JEM 120 transmission electron microscope (TEM). The technique was used to identify (1) the phase of the Cu_xS produced on single crystal substrates[5], (2) the phase of deposited CdS films and (3) the degree of preferred orientation of the crystallites in these films. The major advantage of this technique is that it is non-destructive. Moreover a very short time only is needed to obtain information which allows any structural changes produced by different treatments at various stages of the experiment to be monitored.

In the RHEED technique an electron beam with energy in the range of 10 to 100 keV produces diffraction effects from atomic planes at the surface

of crystalline specimens. If the Bragg diffraction requirement is fulfilled, then

$$\lambda = 2d_{hkl}\sin\theta \qquad (4.1)$$

where the wavelength, λ, depends on the accelerating voltage (and varies from 0.12 to 0.04 Å in the energy range from 10 to 100 keV). d_{hkl} is the interplanar spacing and θ is the Bragg angle between the incident beam and the atomic planes. The interplanar spacing is of the order of Angstroms (Å), so that to obtain a diffraction pattern the Bragg angle must lie in the range from 0.5 to 1.5°. A schematic diagram illustrating the necessary geometrical relationship between the electron beam and the specimen for diffraction to occur is shown in Fig 4.3. Each real space plane (hkl) gives rise to a reciprocal lattice point which has the same set of Miller indices. Each reciprocal lattice point lies on a line which passes through the origin of reciprocal space and which is perpendicular to its corresponding plane in real space. The reciprocal lattice point is situated at a distance from the origin which is inversely proportional to the interplanar spacing d_{hkl}. The condition for constructive interference between diffracted beams is satisfied when a reciprocal lattice point intersects the reflecting sphere in the Ewald sphere construction (see Fig 4.4).

It is usual for a number of reciprocal lattice points to intersect the reflecting sphere simultaneously, particularly when the incident beam lies along a low index direction in the crystal and this leads to the formation of an electron diffraction pattern. In polycrystalline material the random orientation of individual grains results in the formation of rings instead of individual discrete spots. For small values of Bragg angle the relationship $\lambda L = R_{hkl}\ d_{hkl}$ can be derived from the Bragg's condition for constructive interference (see Fig 4.3). This is the camera equation for

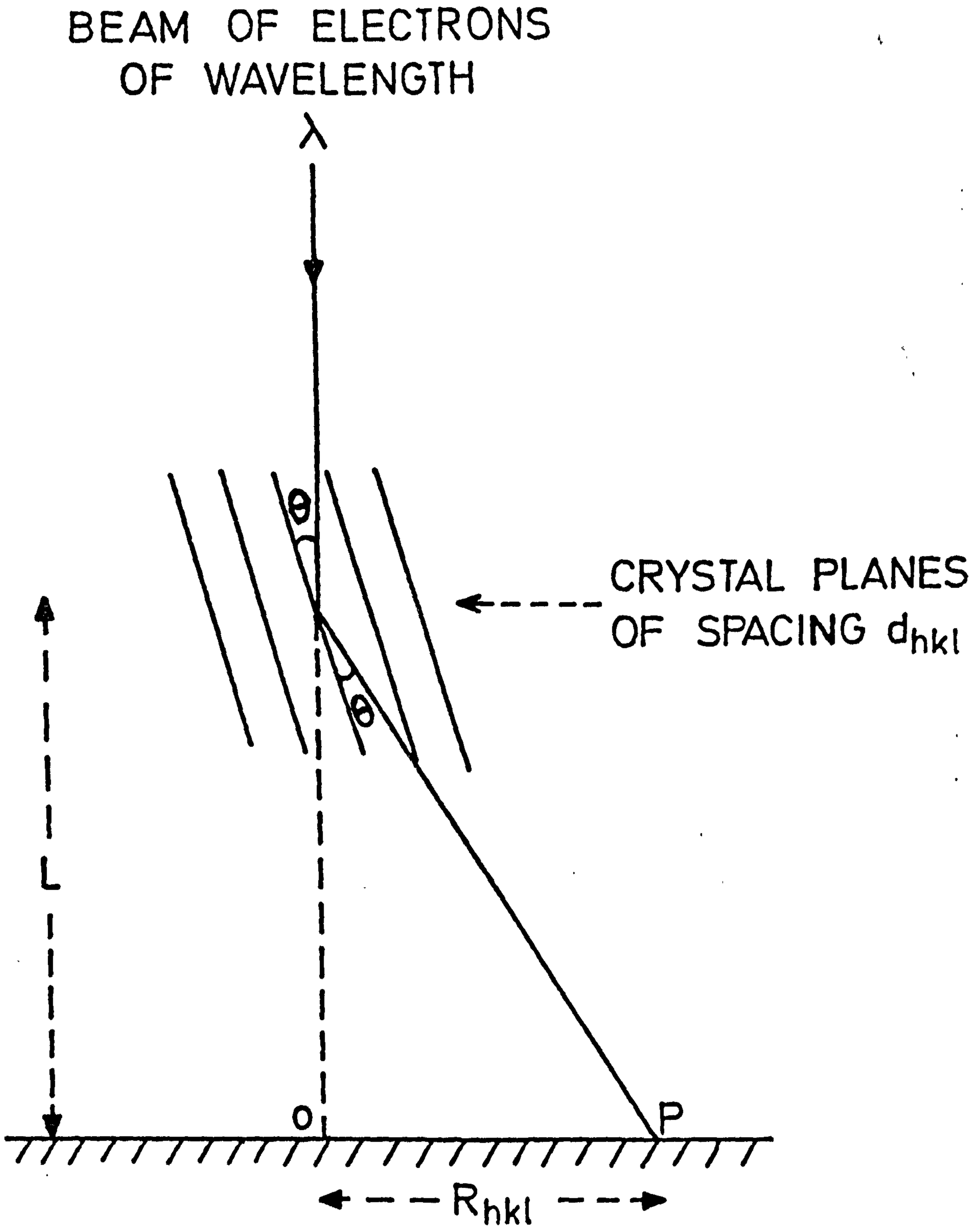


FIGURE 4.3: Schematic diagram illustrating the RHEED technique

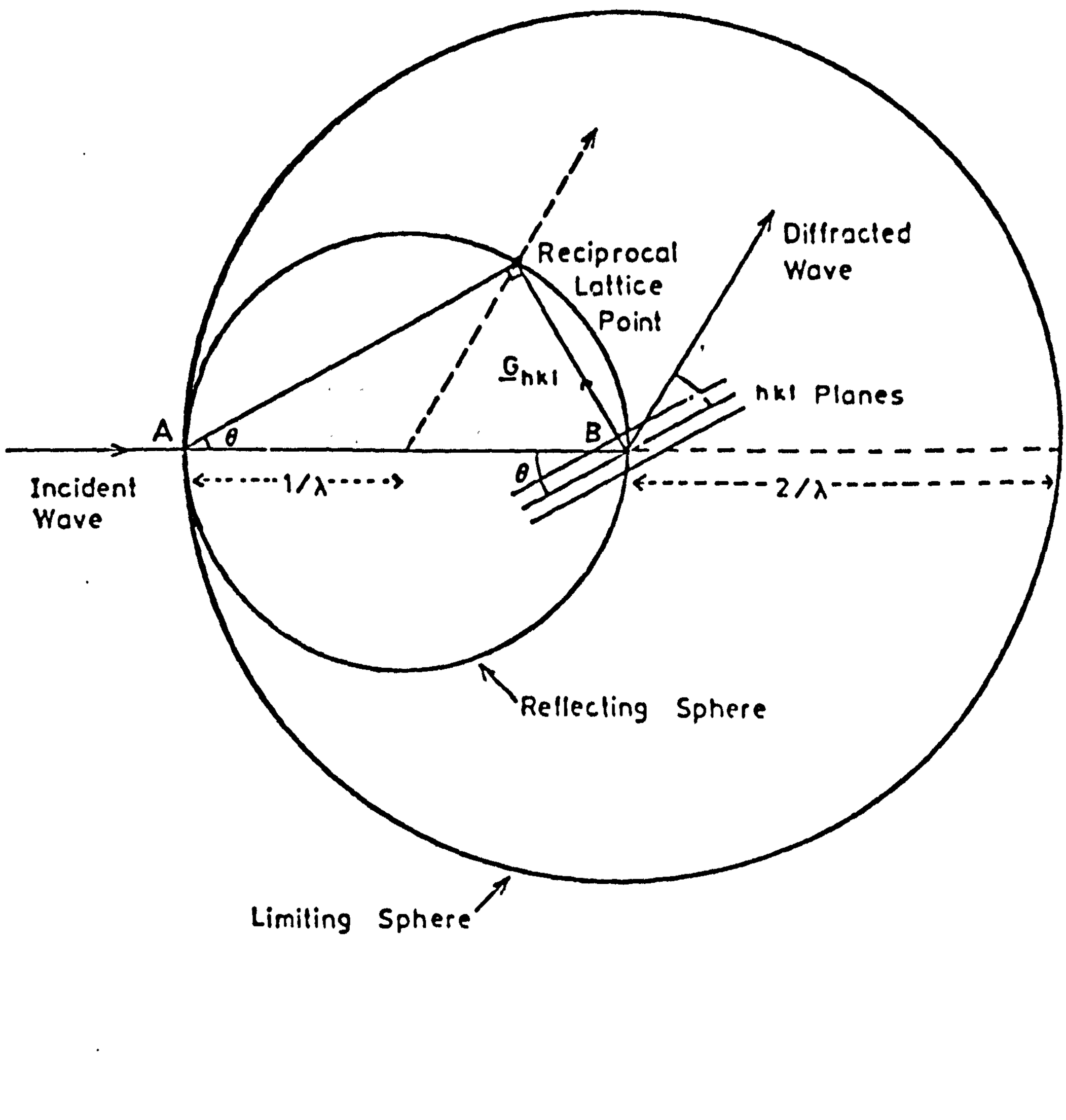


FIGURE 4.4: Ewald's sphere construction

the electron microscope and is used to calculate the interplanar spacings (d_{hkl}) from the observed diffraction pattern. A detailed account of the practical applications of the RHEED technique in the study of wide range of materials has been given by Russell[6].

As the RHEED patterns which were obtained from many of the electrophoretically deposited films after various treatments indicated the presence of a mixture of cubic and hexagonal phases of CdS, efforts were made to measure the intensities of some of the diffraction rings. To achieve this, a Hilger and Watts microdensitometer was employed to provide a graphical representation of the relative intensities of the diffraction rings.

4.5 SCANNING ELECTRON MICROSCOPY

The surface topographies of both single crystals and films of CdS and $Cd_{1-y}Zn_yS$ were investigated using a Cambridge Stereoscan 600 scanning electron microscope (SEM). The cross sections of some films were also studied to assess the film thickness and the degree of grain and columnar growth.

A schematic drawing of the SEM is shown in Fig 4.5. The basic principle of operation is that an electron beam is scanned across the sample in a raster, and the secondary electrons that are emitted from the sample surface are collected by an Everhart-Thornley (ET) detector consisting of a scintillator and photomultiplier (PM). The output from the photomultiplier is taken through the PM tube amplifier and is fed into the input of the cathode ray tube (CRT) monitor which is scanned with the same generator as that used to scan the electron beam across the sample. In this way a micrograph of the secondary emitted electrons from the specimen surface is generated.

The SEM may be operated in several different modes by imaging various signals derived from the different interactions that occur between the electron beam and the specimen[7]. These are illustrated in Fig (4.6). In most of the work reported here, the secondary emission (SE) mode was used. However silk screen printed films of CdS and $Cd_{1-y}Zn_yS$ were examined in the Absorbed Current

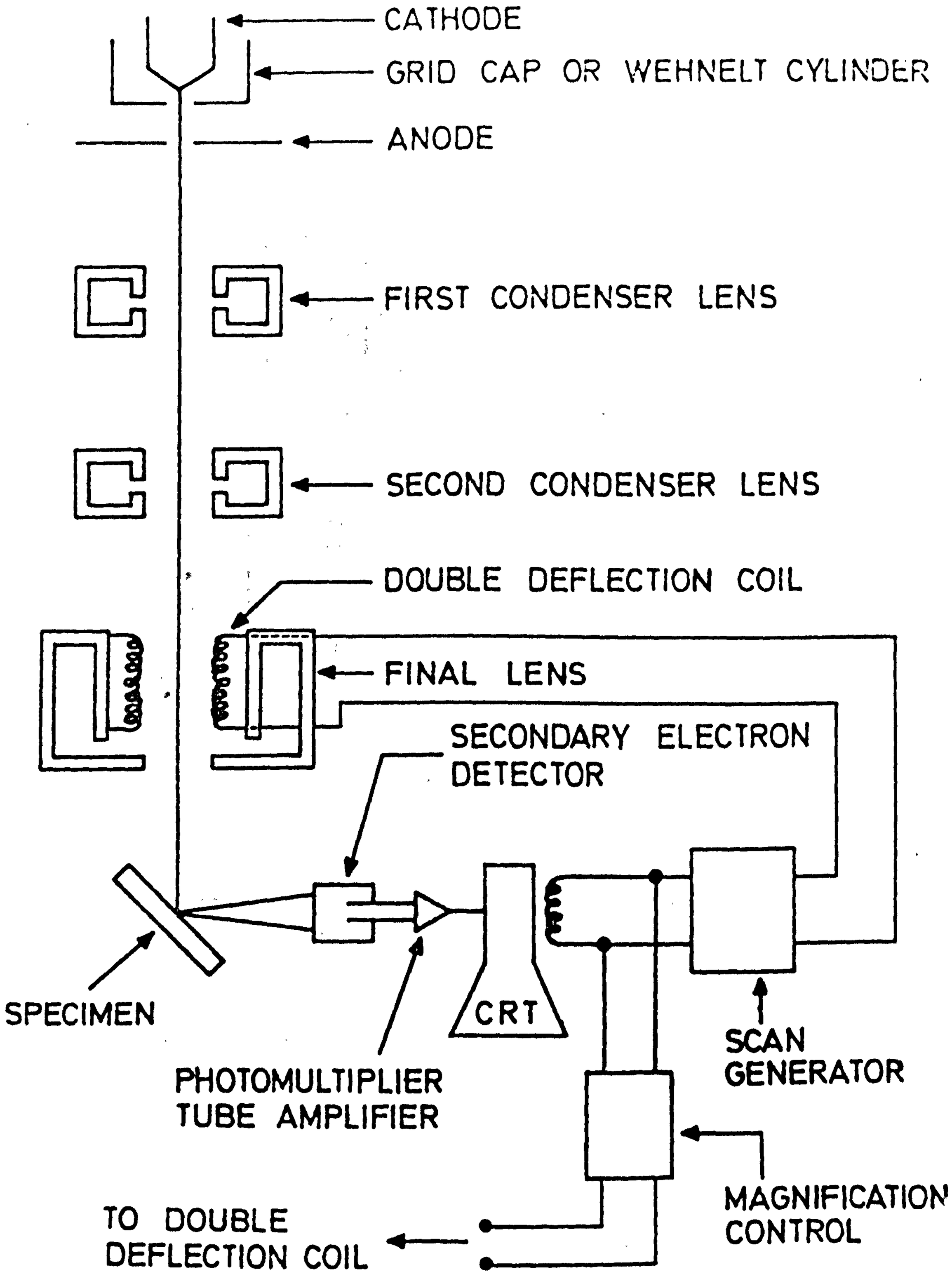


FIGURE 4.5: Schematic diagram of the SEM.

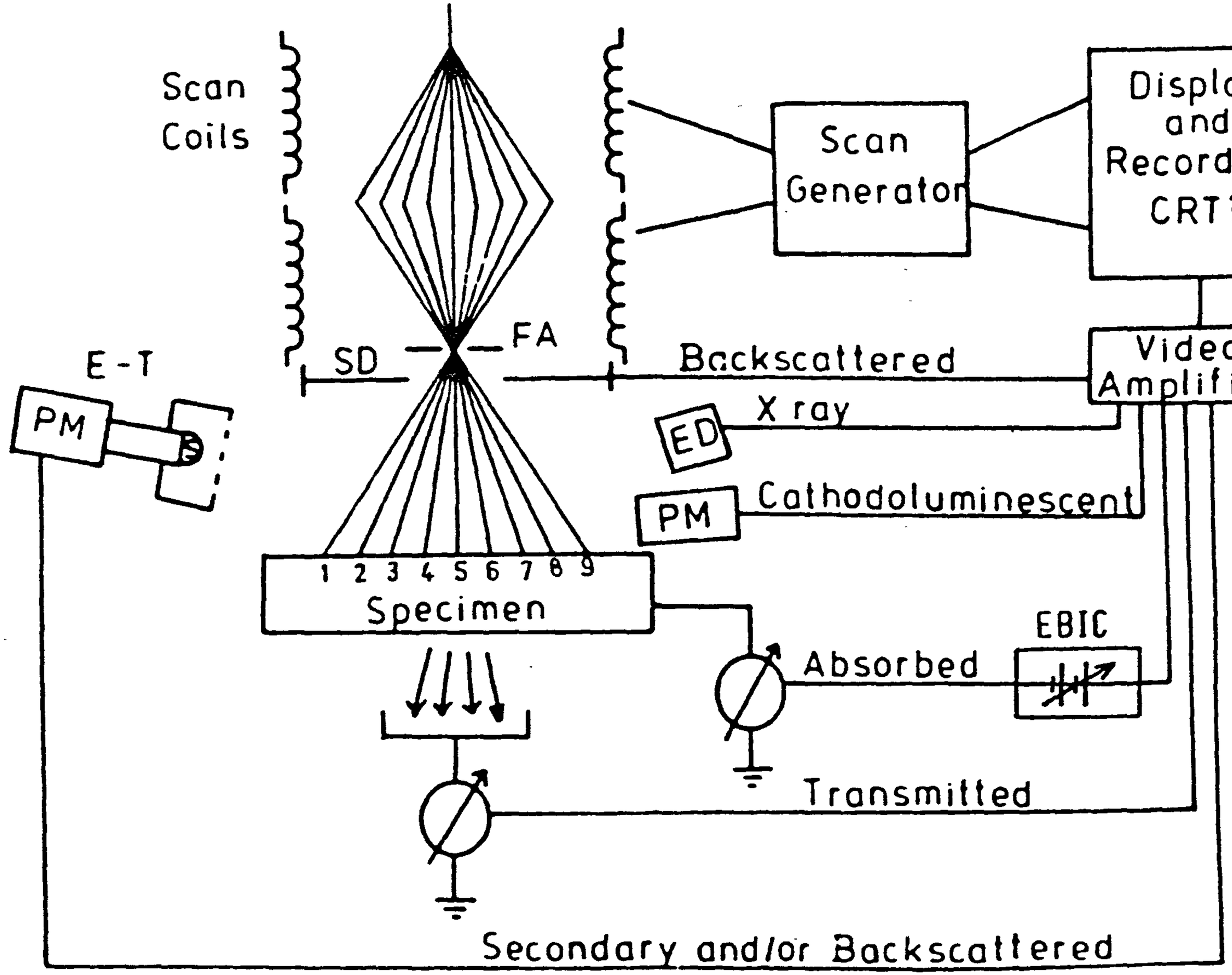


FIGURE 4.6: Schematic diagram showing the various modes of operation of the SEM.

mode. For elemental analysis of certain surfaces the technique of energy dispersive analysis by x-rays (EDAX) was employed using a Link systems 860-series 2 Analyser.

For the SEM examination of material deposited on to glass substrates (e.g. thermally evaporated and electrophoretically deposited film) samples were sputter coated with gold to provide a conducting path to avoid charge build-up.

4.6 MEASUREMENT OF CURRENT-VOLTAGE CHARACTERISTICS

Current-voltage characteristics were recorded in the dark and under AM 1 illumination at room temperature. Simulation of AM 1 illumination was accomplished using a 1.5 kW quartz halogen strip lamp with a parabolic reflector housing, and a tray of water 2 cm deep acting as a filter to reduce the infrared content (Fig 4.7). The source was calibrated using a standard silicon PIN diode (type 10 DF, United Detector Technology) and adjusting the distance between the source and the sample. Measurements of the current-voltage characteristics were carried out point-by-point using a high impedance Bradley voltmeter (type 173 B) and a low impedance Hewlett Packard ammeter (type 3465 B). The bias voltage was provided by DC voltage calibrator type 2003 (Time Electron Ltd). An automated current-voltage tracer employing an X-Y plotter was also used to monitor the effects of different treatments.

4.7 MEASUREMENT OF SPECTRAL RESPONSE

The spectral sensitivity of cells was measured using light from the exit slit of a Barr and Stroud double prism monochromator, type VL 2, fitted with spectrosil 'A' silica prisms. A 250 watt quartz halogen lamp driven by a 200 V d.c. stabilised power supply was used as the light source. The energy distribution of the source at the exit slit, which includes the varying dispersion of the prism monochromator, was measured using a Hilger and Watts Schwartz compensated linear vacuum thermopile, type FT 16 301/60297. The input from the tungsten lamp at the entrance slit to the monochromator

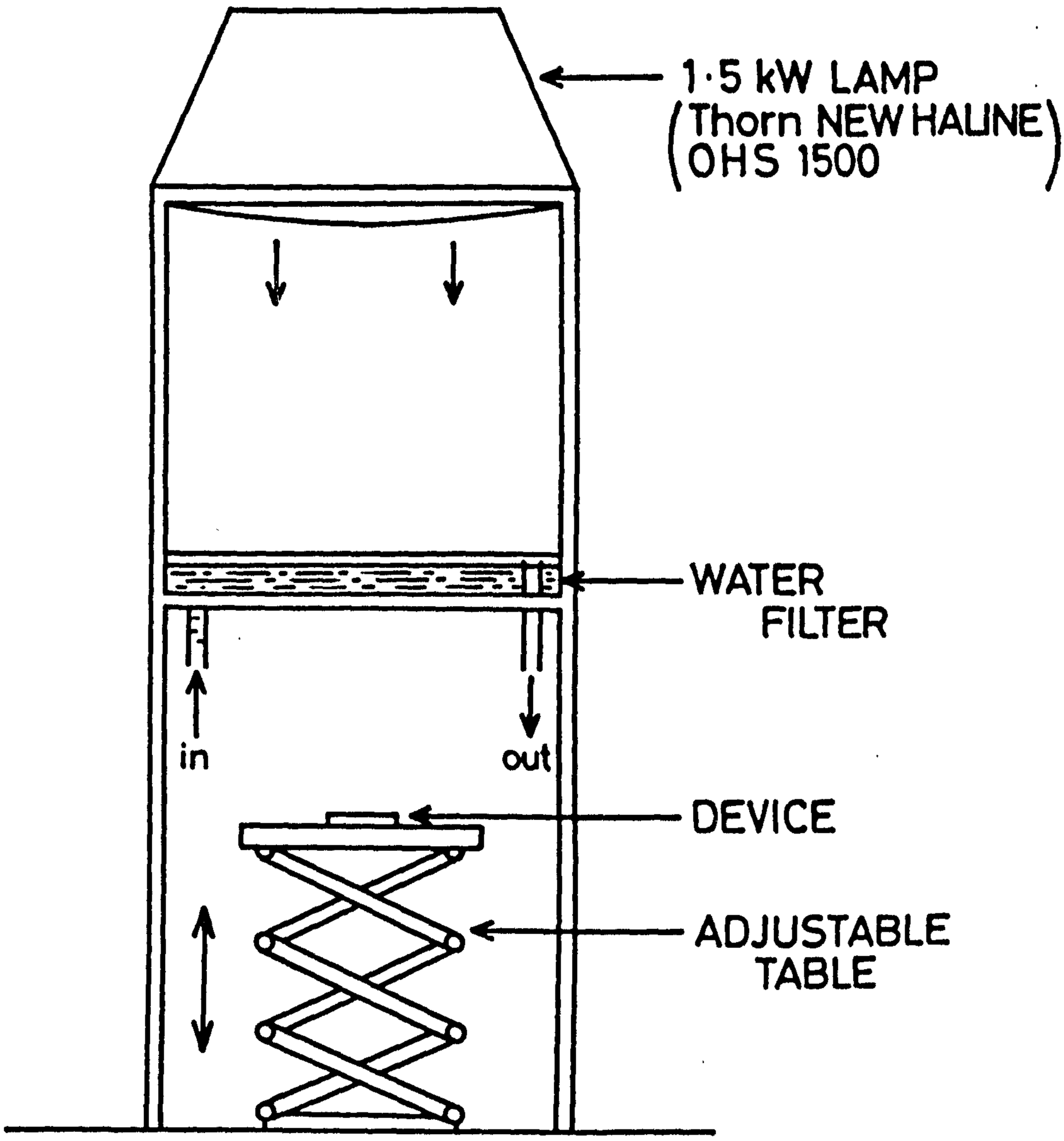


FIGURE 4.7: Solar Simulator for AM 1 illumination

was mechanically chopped at 10 Hz and the resulting output of the thermo-pile was fed to a lock-in amplifier type 9401,via a Nanovolt preamplifier, type 431.

A schematic diagram of the arrangement used for the spectral response measurements is shown in Fig 4.8. The monochromator was periodically calibrated with a sodium lamp source to avoid any effects of wavelength drift in the monochromator. The device under test was mounted in a cryostat where its temperature was monitored using a copper constanton thermocouple. It was illuminated from the front on the Cu_xS surface in the front wall mode. A second window was provided in the cryostat for bias illumination when required. The photocurrent and voltage were measured using a Keithley Electrometer model 602 which has a high impedance for voltage measurements and very low input impedance for current measurements. Consequently, the recorded spectra of photovoltage and current were adequate approximations of the open circuit-voltage and short circuit current. The output of the electrometer was plotted on a Honeywell Electronic (model 196) high impedance chart recorder.

4.8 MEASUREMENT OF JUNCTION CAPACITANCE

Capacitance measurements were made at 1 MHz using a Boonton 72 B capacitance meter. C-V characteristics were measured point-by-point by applying the bias voltage through a D-C calibrator type 2003 Some C-V characteristics were recorded using an integrated circuit voltage ramp which allowed the scan rate to be adjusted from 1 sec/volt to 1000 sec/volt. The output was measured with a Hewlett Packard X-Y-T recorder model 7041A.

For photocapacitance measurements, the dark capacitance of each device was compensated to allow small changes induced by the monochromatic irradiation to be recorded. The output of the capacitance meter was connected to a Honeywell chart recorder. A schematic diagram of the arrangement used for these photocapacitance measurements is shown in Fig 4.9. For steady state photocapacitance studies the temperature of the device was lowered to 85 K to minimize thermal effects. As the temperature was reduced, the capacitance

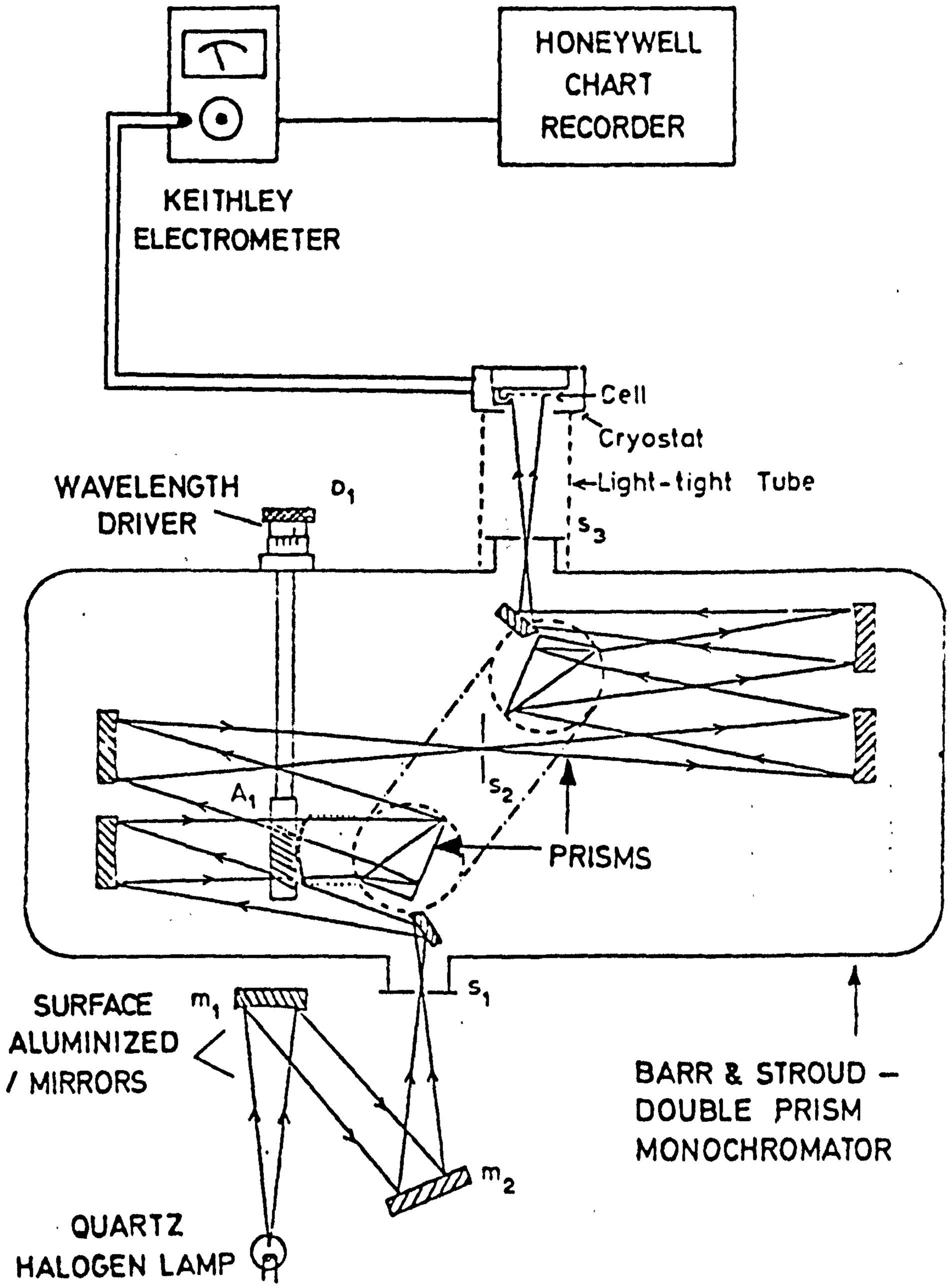


FIGURE 4.8: Experimental arrangement used for spectrul response measurements.

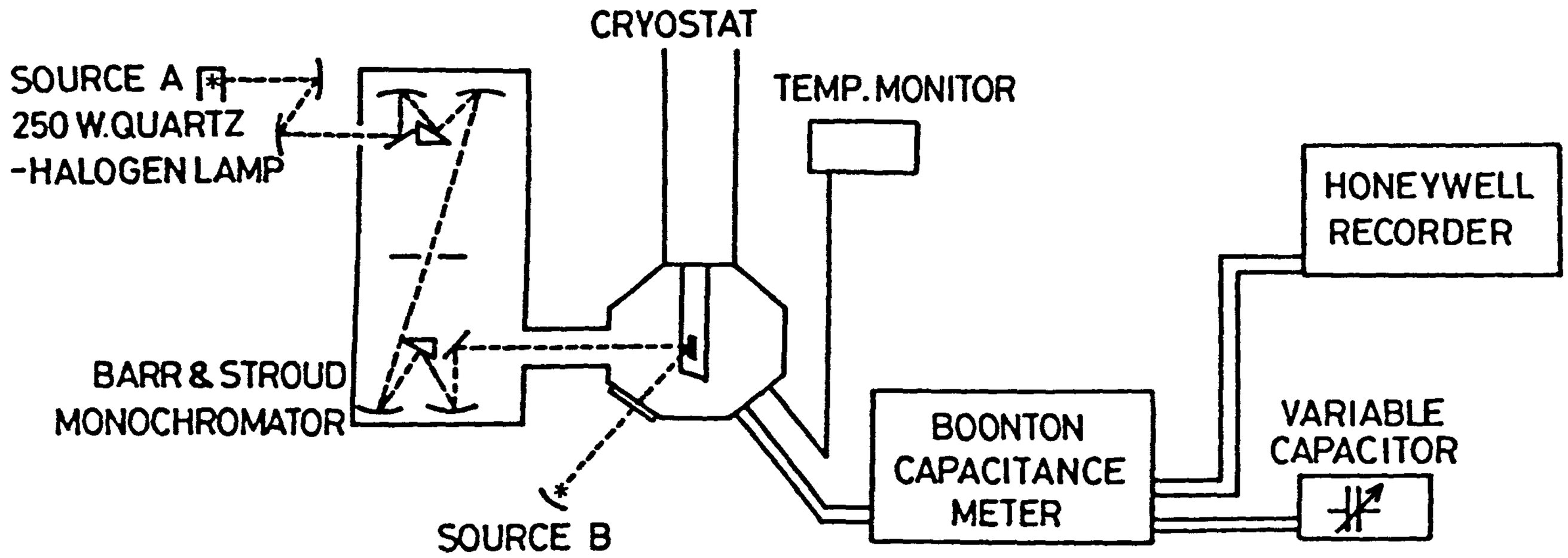


FIGURE 4.9: Experimental arrangement used for photocapacitance measurements.

decreased. In all experiments sufficient time was allowed to achieve steady state values. The wavelength of the incident light from the monochromator was scanned very slowly from long to short wavelengths.

In the transient measurements, particularly for the infrared quenching of the photocapacitance, two sources were employed. The second source used in addition to light from the monochromator (which is referred to as the primary source in this measurement) was also a quartz halogen lamp powered by a 24 d.c. supply. An Oriel 5200 Å band pass filter was used with an infrared absorbing filter in the window. The exposure of the sample to the monochromator light was controlled with a chopper. The details of the experiment are discussed in section 6.2 of Chapter 6. The quenching and recovery capacitance transients when the secondary light was switched on and off were measured using the chart recorder with increased speeds (10-20 secs. per inch).

4.9 MEASUREMENT OF SERIES RESISTANCE

The series resistance was measured by the flash lamp technique developed by Chaffin and Osbourn[8]. The light source used was an inexpensive flash unit (SUNPAK AUTO 33). The light intensity was varied by changing the distance between the solar cell and the flash unit. The cell output was measured by means of a Telequipment storage oscilloscope type DM-64. At low levels of intensity, the cell responded to the actual temporal characteristics of the flash unit. As the intensity was increased, the total cell current began to saturate. In this region the peak cell current changed logarithmically with light intensity. Measurements of the output voltage with the illumination were made with two different load resistors and the series resistance was determined from equation 3.28 (see section 3.6, Chapter 3). A variable resistance box type A-6-A (Muirhead & Co.Ltd) was used to apply small load values. A schematic diagram of the arrangement used for this measurement is shown in Fig 4.10.

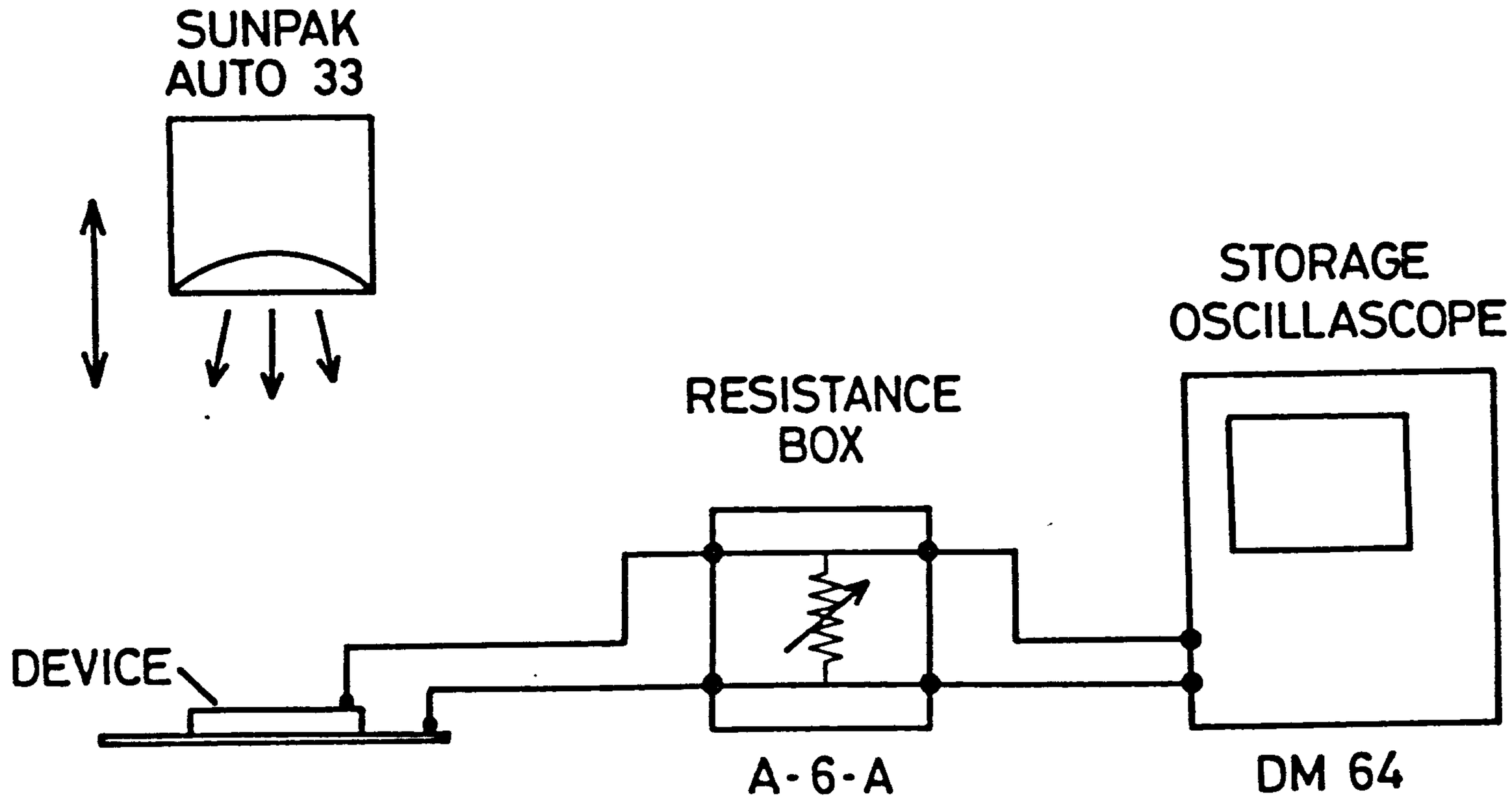


FIGURE 4.10 : Experimental arrangement used for series resistance measurements

REFERENCES TO CHAPTER 4

1. L. Clark and J.Woods, Brit.J.Appl.Phys. 17 (1966) p.319.

2. L.Clark and J. Woods, J.Crystal Growth 3 (1968), p.126.

3. B.G. Caswell, Ph.d. Thesis, University of Durham, 1976.

4. S. Oktik, Ph.D. Thesis, University of Durham, 1982.

5. G.J.Russell and J.Woods, Phys. Stat.Solidi (a) 46 (1978) p.433.

6. G.J.Russell, Prog.Crystal Growth and Charact. 5 (1982) p.291.

7. J.I.Goldstein (Ed) and H. Yokowitz (Ed): Practical Scanning Electron Microscopy (Plenum Press, New York, 1975).

8. R.J. Chaffin and G. C.Osbourn : Appl.Phys. Lett. 37 (1980), p.637.

CHAPTER 5

OPTIMISATION OF THE DRY BARRIER PROCESS

5.1 INTRODUCTION

In this Chapter the effects of different preparational parameters on the device characteristics are discussed in detail, with a view to optimising the dry barrier process for the formation of the chalcocite phase of Cu_xS on CdS in the fabrication of CdS-Cu_xS heterojunctions. In the course of the work, many CuCl films of different thicknesses were systematically deposited on the CdS dice using a range of deposition rates and substrate temperatures. The ultimate behaviour of the devices has been correlated with different aspects of the preparative procedure. Measurements of current-voltage characteristics in the dark and under AM 1 illumination, spectral responses, RHEED and SEM studies were used to evaluate the effect of the preparational parameters on the performance of the devices. In addition, post preparative heat treatments in different ambients were carried out to optimise the device characteristics. Further, the effect of heat treatments on the series resistances was studied using a flash lamp measurement technique (see Section 3.6). The spectral responses of the OCV and SCC of the devices before and after heat treatments were measured at different temperatures. The effect of temperature and bias light on the different regions of spectral response was used to distinguish between the response due to the chalcocite and djurleite phases and that due to copper centres.

5.2 STRUCTURAL ASPECTS OF THE HETEROJUNCTION

5.2.1 The Topography of the Etched Surface

The devices were fabricated on dice with dimensions of $4x4x2mm^3$ cut from large single crystal boules of CdS grown in this laboratory using the technique described in Chapter 4, Section 4.2. The single crystal boules were first oriented using X-ray back reflection techniques and were

then cut into slices 2 mm thick with the c axis perpendicular to the large area faces. Some of these slices were mechanically polished by hand on a polishing pad, and others were polished on a lapping machine. The normal practice was to start polishing with alumina powder of 5 μm particle size, so that the major damage created on the surface by the diamond saw during the cutting process was removed. The grain size of the alumina powder was then reduced to 3 μm and finally to 1 μm to finish with a smooth surface. Dice ($4 \times 4 \times 2mm^3$) were obtained by cutting these polished slices. The oriented, polished dice were washed thoroughly in sequence with acetone, methanol, isopropyl alcohol and water to remove grease or oil from the surface.

In general these dice were etched in Conc.HCl for 20 secs to remove the polycrystalline work damaged layers formed during the mechanical polishing process[1]. Etching also enabled the two polar faces to be distinguished[2]. After etching in Conc.HCl the sulphur face ($00\bar{1}$) appeared optically matt while the cadmium face became polished and highly reflective. The surfaces of etched samples was examined in a Cambridge S600 scanning electron microscope. The etched ($00\bar{1}$) surfaces of a few samples were characterised by the presence of large hillocks (see Fig 5.1), but those of others were less regular, appearing to possess a spongy surface (Fig 5.2). Care was taken to carry out the experiments on samples with similar topography during a study of a particular set of parameters and their effect on the device characteristics.

5.2.2 Heterojunction Formation

Indium contacts were made by pressing a 1mm pellet of indium wire (0.5 mm thick) on to the cadmium face of a die and then heating in an argon atmosphere at $200^{o}C$ for 10 minutes to melt the indium. In this way an excellent ohmic contact was achieved[3]. In a few cases where the heterojunctions were deliberately formed on the Cd face of CdS, the ohmic contacts were provided on the sulphur face. After the formation of ohmic contacts,

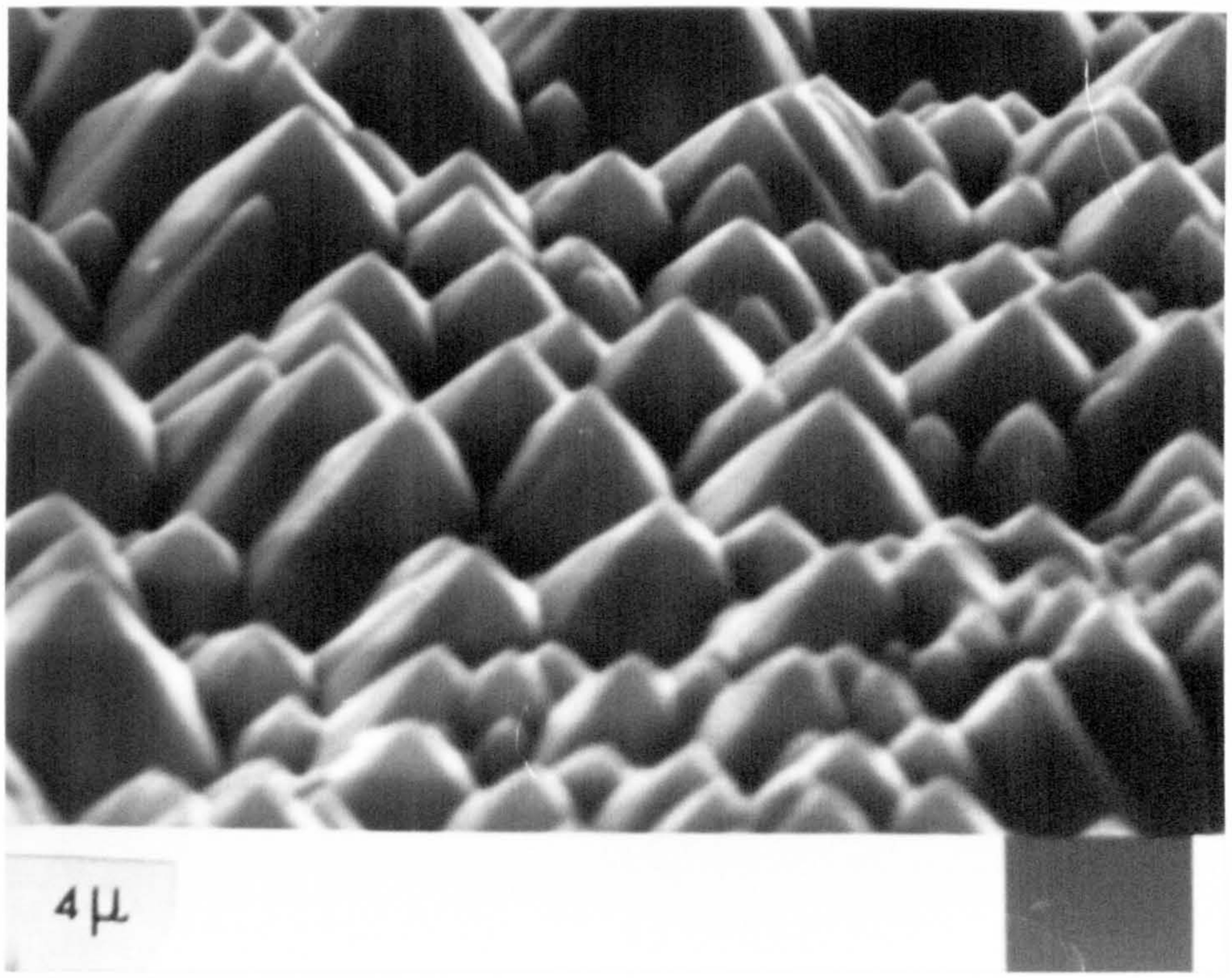


FIGURE 5.1: Secondary emission micrograph of etched (00$\bar{1}$) single crystal CdS surface comprising large faceted hillocks.

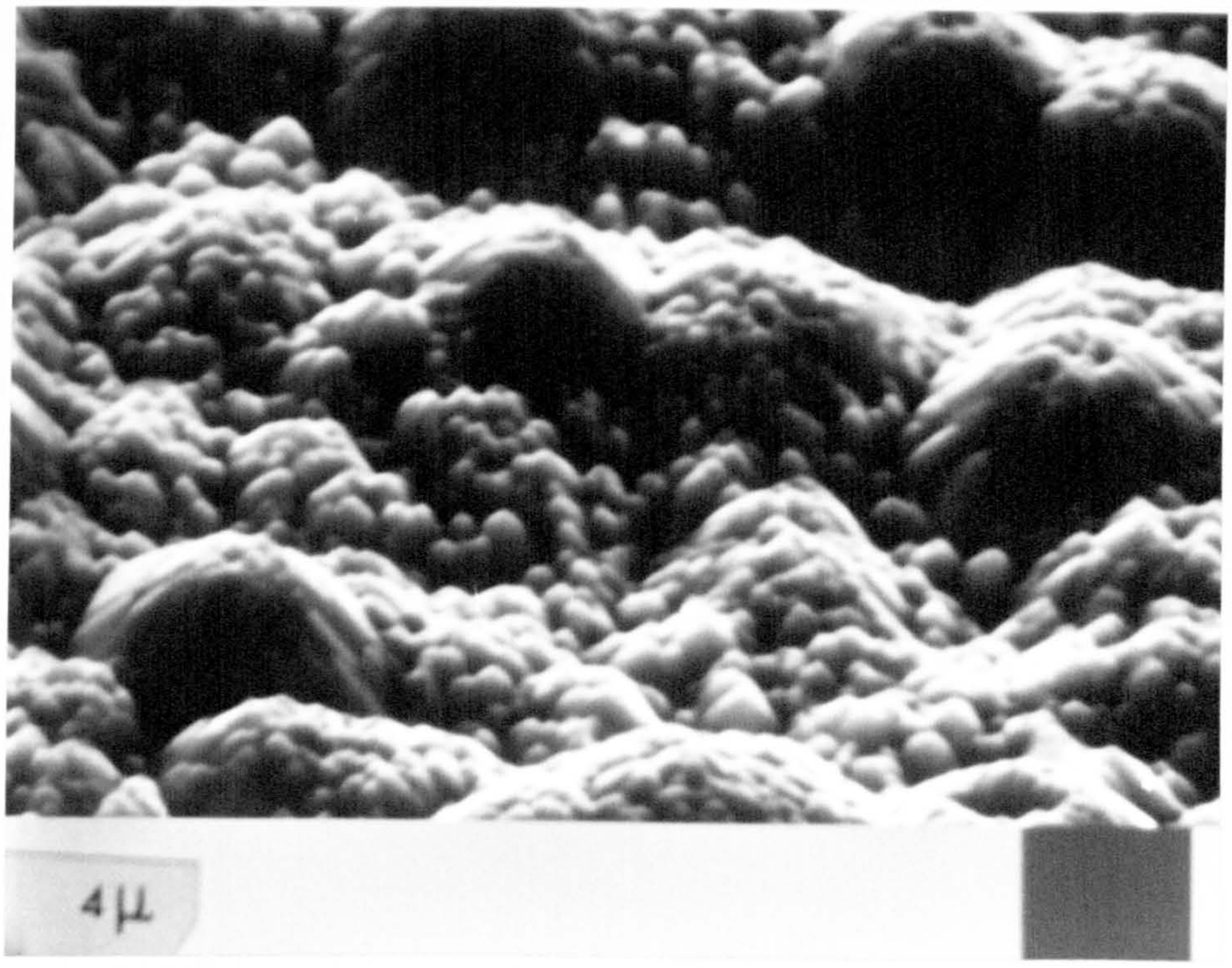


FIGURE 5.2: Secondary emission micrograph of etched (00$\bar{1}$) single crystal CdS surface comprising small rounded hillocks.

all dice were etched again for 10 secs in Conc. HCl in order to remove any oxide layer that might have formed. Dice were washed and dried in a stream of nitrogen and then placed inside the vacuum evaporator (see Section 4.3, Chapter 4) for the deposition of CuCl on to the sulphur face. The Analar CuCl (green in colour) was bleached thoroughly with $\frac{1}{10}$N HCl, to reduce any cupric ions present to cuprous ones, since the evaporation of any cupric chloride would result in the formation of a copper deficient phase of copper sulphide adversely affecting the device performance[4,5,6]. For each evaporation a charge of 1.5 gm of bleached CuCl was used. The junction area on each dice was defined by a 3mm diameter hole in a mask held firmly against the face of the dice. The substrate temperature, charge temperature, evaporation rate , and the thickness of CuCl were measured during each evaporation. A number of different thicknesses were deposited systematically using a range of substrate temperatures and deposition rates. To limit the number of permutations, each of the parameters was varied in turn while keeping the other two constant. After depositing the CuCl layer the samples were allowed to cool down inside the vacuum chamber. They were subsequently heated at 200°C for 1 to 10 minutes in a stream of argon, to promote the solid state reaction between CuCl and CdS resulting in the formation of a topotaxial Cu_2S layer[4]

$$CdS + 2\,CuCl \longrightarrow Cu_2S + CdCl_2$$

The $CdCl_2$ by-product of the reaction was washed away using absolute alcohol. The Cu_xS layer thus produced was examined by RHEED.

5.2.3 The Copper Sulpide Layer

In the solid state reaction the Cd^{2+} ions are displaced by Cu^{+} ions while the S^{--} ions of the CdS substrate remain substantially immobile[4]. The p-type copper sulphide layer thus formed is the main optical absorber

and current generator in the CdS-Cu_xS solar cell[7]. For efficient conversion of the incident solar energy, it has been claimed that the phase of Cu_xS should be chalcocite[4,8,9,10]. However, in general a mixture of the copper deficient phases djurleite ($Cu_{1.96}S$), digenite ($Cu_{1.8}S$) and covellite (CuS) have been found to co-exist with the chalcocite[10,11,12]. Devices with a copper deficient phase of Cu_xS lead to a loss of efficiency[7]. The main aim of this work was to optimise the preparative conditions in an attempt to produce the chalcocite phase of Cu_xS using the dry barrier process.

5.2.4 RHEED Investigations

To check the phase of Cu_xS produced, samples were examined in reflection high energy electron diffraction. This technique (see Section 4.4, Chapter 4), has been used earlier by many workers to identify the phase of copper sulphide[13,14,15,16]. The main advantage is its non-destructive nature.

A good example of pure chalcocite was obtained from the samples which were prepared using a deposition rate of 400 Å/min to produce a film 0.15 μm thick on a substrate held at 35°C, and subsequently heated to 200°C for 2 minutes in argon to complete the process. The RHEED patterns from this particular sample taken with the beam lying parallel to the [100] and [120] directions in the CdS are shown in Fig 5.3(a) and Fig 5.3(b) respectively. The patterns can be indexed as arising from the [100] and [010] zone axes of the orthorhombic unit cell of chalcocite respectively[16]. As the c axis of the CdS coincides with the a axis of chalcocite during the growth of the Cu_2S layer[4,17], it leads to the topotaxial formation of unit cells with three possible orientations of the orthorhombic chalcocite on the sulphur sublattice of the hexagonal CdS (Fig 5.4). When the beam is incident along a [100] axis of one unit cell (labelled as M), it is also incident along a [430] direction in each of the unit cells labelled L and R. Similarly when the electron beam is incident along the b axis [010] of the unit cell M, it is simultaneously incident along a [410] direction in the

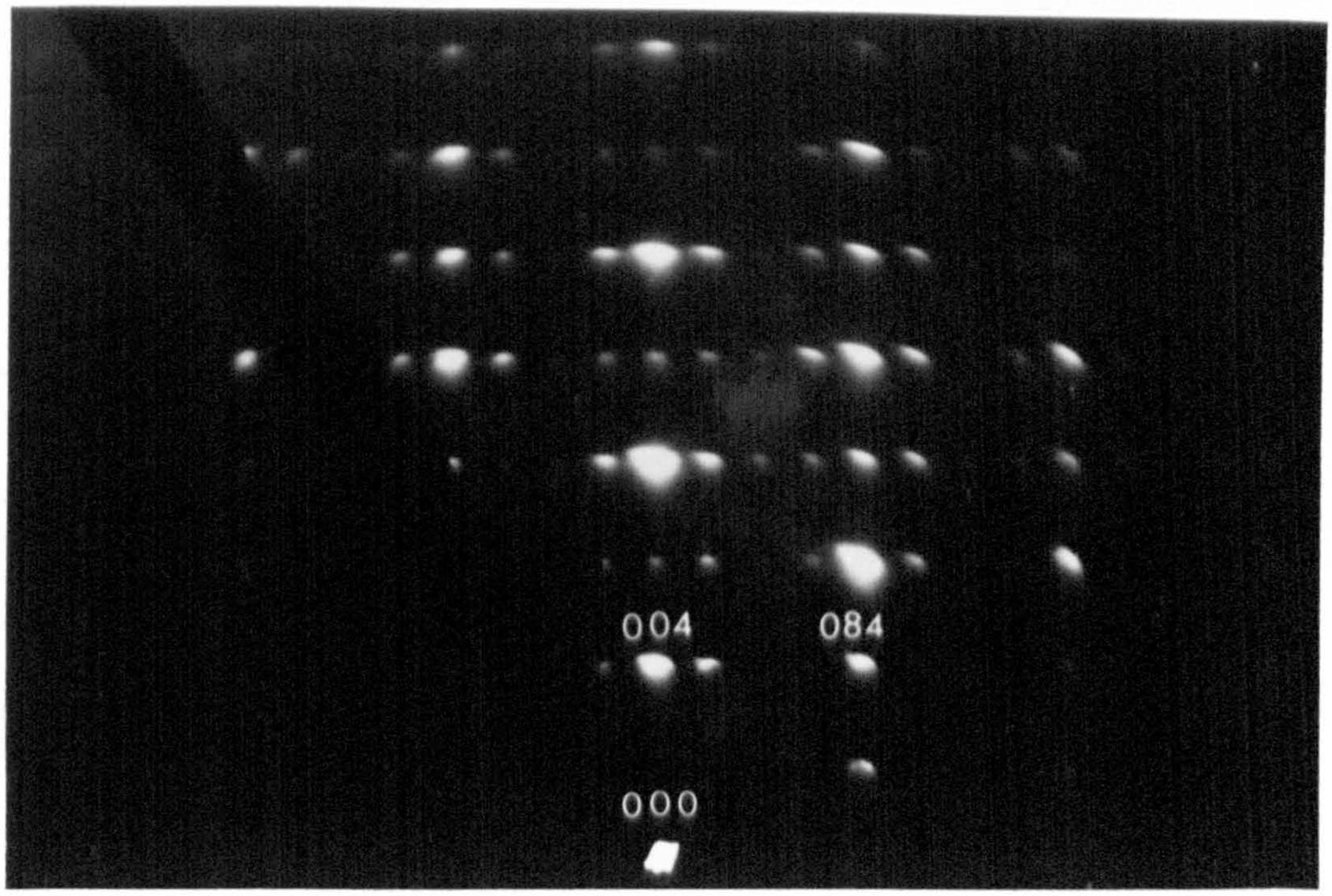


FIGURE 5.3(a): RHEED pattern of chalcocite along [100 direction of CdS.

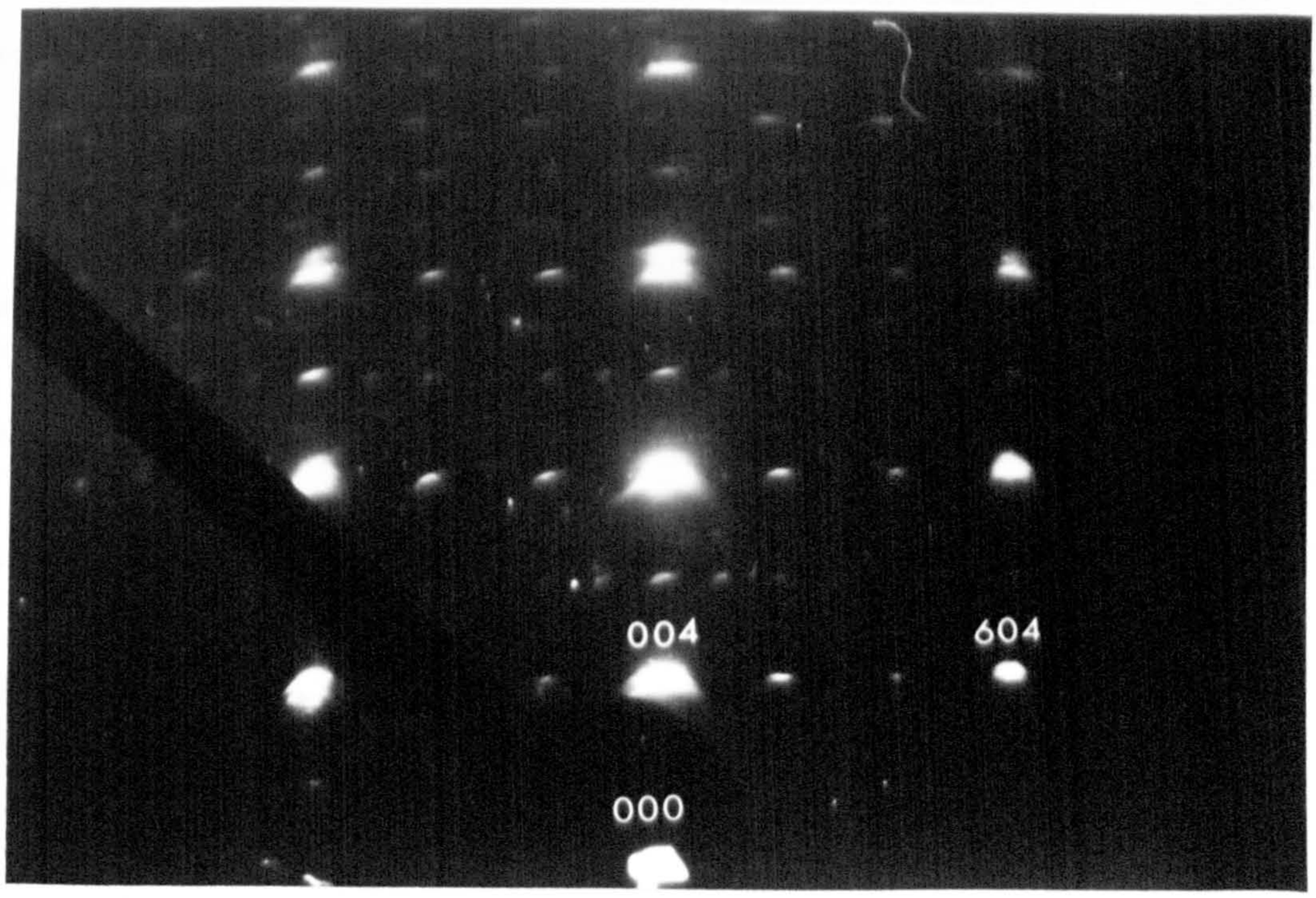


FIGURE 5.3(b): RHEED pattern of chalcocite along [120] direction of CdS.

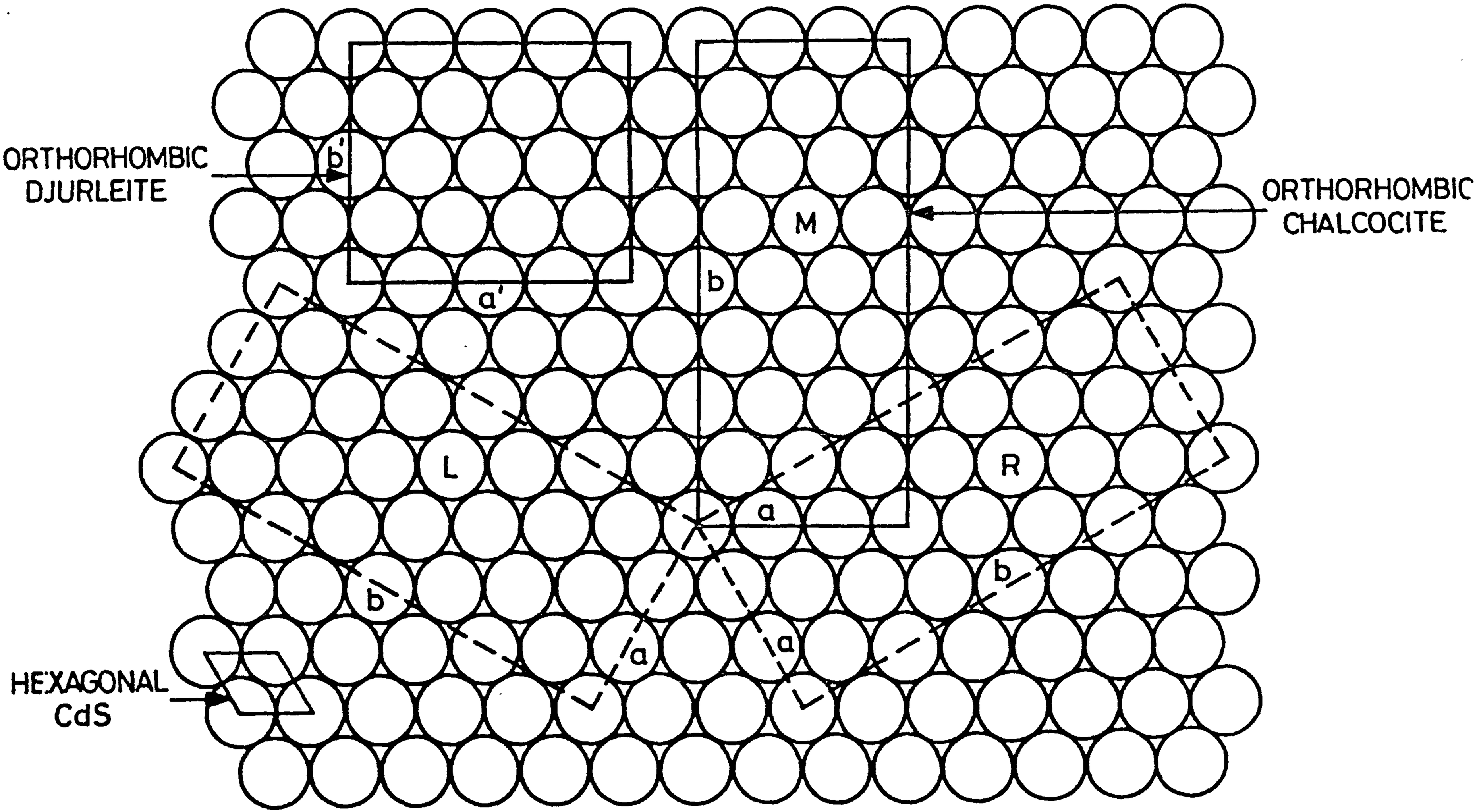


FIGURE 5.4: Unit cell geometries of chalcocite (in three orientations) and djurleite in the basal plane of CdS.

unit cells L and R. The two reflections from the two different zone axes are coincident within experimental error[16]. Thus even though the patterns in Fig 5.3(a) and 5.3(b) arise from three different grains of chalcocite, they appear as single crystal spots. The coincident diffraction beams from grains in each of the possible orientation and from the CdS accounts for the relatively more intense reflections. The six-fold symmetry of CdS leads to identical diffraction patterns on rotating the sample by 60°.

A good example of pure djurleite is shown in Fig 5.5(a) and Fig 5.5(b). This particular sample was produced by depositing a 0.07 μm thick layer of CuCl at 200 Å/min onto a substrate held at 20°C. These RHEED patterns may also be indexed as arising from the [100] and [010] axes of the orthorhombic unit cell of djurleite. The closer spacings of the diffraction spots in the pattern from the djurleite can be explained by the larger spacings of the C planes of this phase.

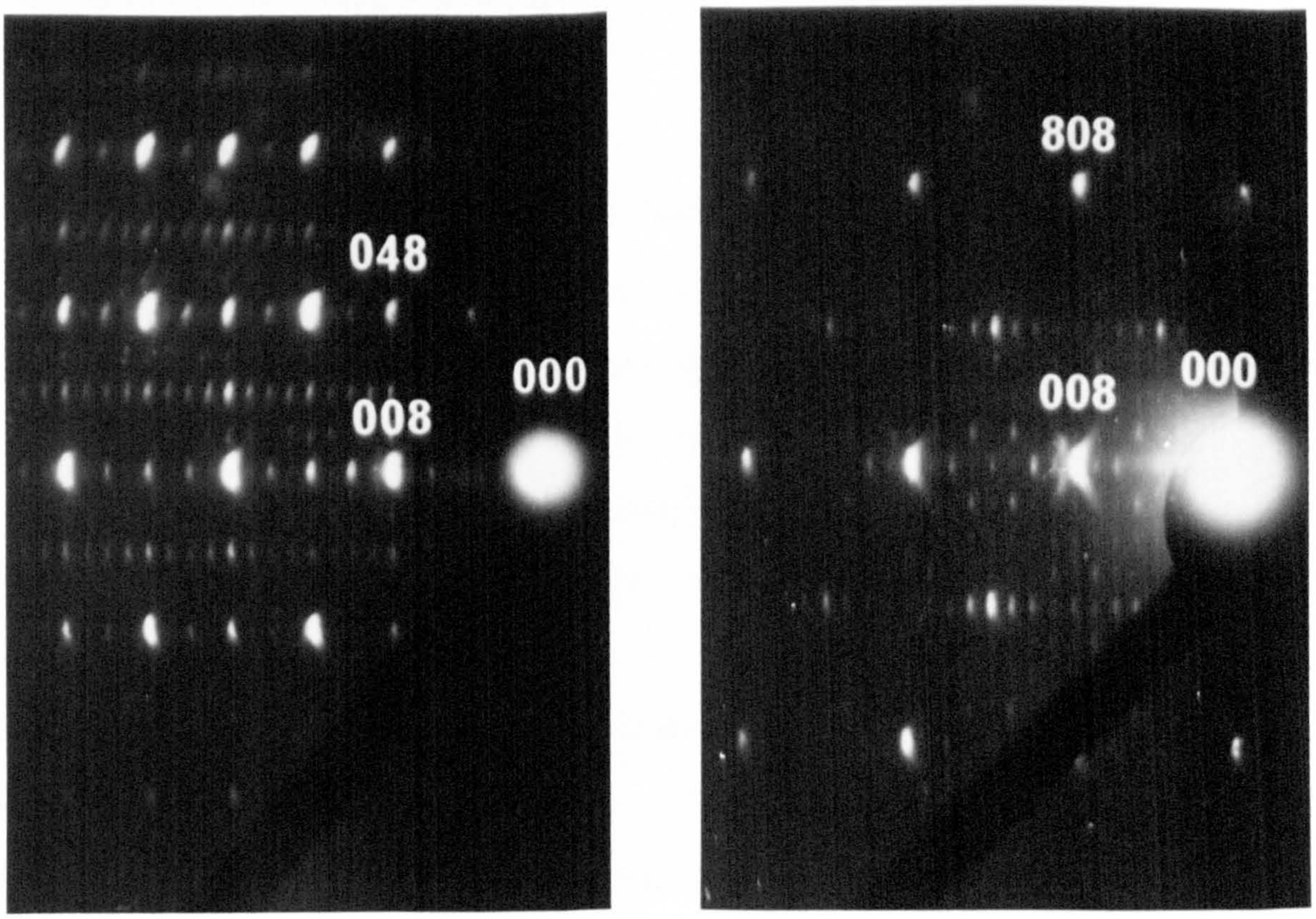
The most frequently observed patterns consisted of a combination of those in Figs 5.3 and 5.5 with different intensities of the diffraction spots. Typical examples are shown in Figs 5.6(a) and 5.6(b) which indicate the presence of a mixture of chalcocite and djurleite. A small amount of the hexagonal phase which normally co-exists with the djurleite phase, and which has the same a axis, is difficult to detect from the RHEED pattern since the diffraction spots associated with the two phase coincides.

After investigating the phase of Cu_xS by RHEED, a circular gold dot, 1 mm in diameter was deposited on to the copper sulphide layer by thermal evaporation to complete the fabrication of the device.

5.3 PROPERTIES OF AS-MADE HETEROJUNCTION

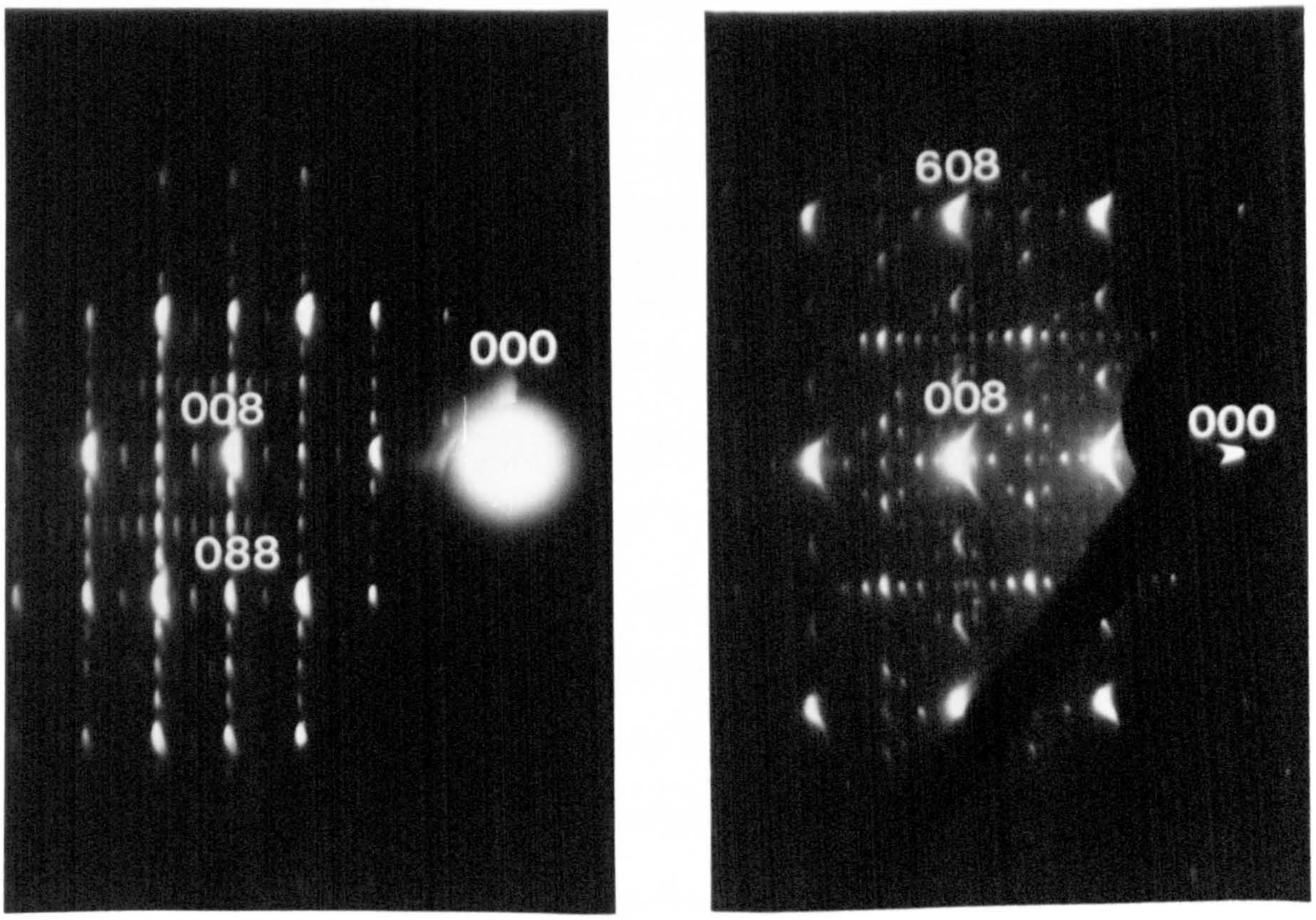
5.3.1 Spectral Response

The spectral response of the OCV of each device was measured using a Barr and Stroud prism monochromator (see Section 4.7, Chapter 4). The measurements were made at various stages to characterise the Cu_xS layer



(a) (b)

FIGURE 5.5: RHEED patterns of djurleite along (a) [100] axis of CdS (b) [120] axis of CdS.



(a) (b)

FIGURE 5.6: RHEED patterns of chalcocite-djurleite mixture along (a) [100] axis of CdS (b) [120] direction of CdS.

and the junction behaviour. Observed features in the spectral response were correlated with the RHEED studies, as has been done previously in this laboratory for cells formed by the wet plating technique[18,19]. Since the samples have to be heated to promote the solid state reaction in the dry barrier process, the spectral response of devices heated for different lengths of time was measured in order to monitor the progress of the reaction.

In this particular set of experiments, 0.2 μm thick layers of CuCl were put down on sulphur faces of CdS at 400 Å/min, while holding the substrate at 35°C. The samples were subsequently heated at 200°C in flowing argon (20 cc/min) for periods ranging from 1 min to 10 min to promote the reaction between the CuCl and CdS. RHEED observations revealed that the chalcocite phase was present in the samples heated for both 1 min and 2 min, while the samples heated for 5 mins and 10 mins contained a mixture of chalcocite and djurleite. The spectral responses of the OCV of these devices are shown in Fig 5.7. The two peaks at wavelengths of 0.96 μm and around 0.75 μm correspond respectively to the absorption of light across the indirect bandgap of chalcocite[20] and across the direct bandgap of djurleite[8]. In the studies of the wet plated junctions[18,19] it was demonstrated that cells with layers of chalcocite had a peak in the spectral response of the OCV at 0.92 μm, while devices with layers of djurleite showed maximum response in a band centred near 0.7 μm. From the curves in Fig 5.7 it is obvious that heating for 2 mins was sufficient for the completion of the solid state reaction and further heating had a deleterious effect on the phase of the copper sulphide. After heating the device for 5 minutes and 10 minutes, the response at 0.96 μm decreased while that at 0.7 μm increased. These observations are consistent with the RHEED patterns where a mixture of the djurleite and chalcocite phase of Cu_xS was revealed. In contrast,

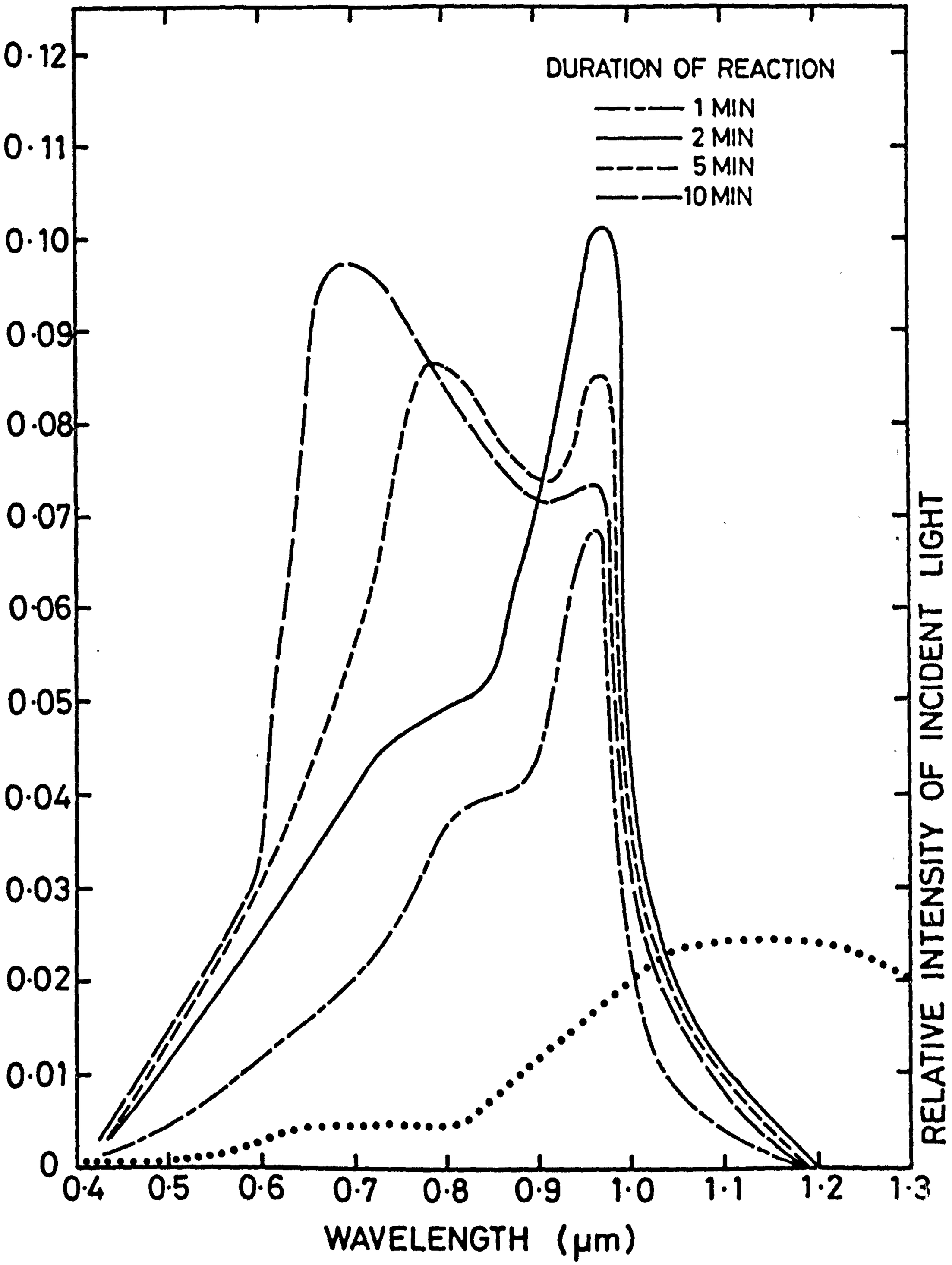


FIGURE 5.7: The effect of duration of the reaction process on the spectral response of as-made devices.

in the sample heated for 1 minute, although the response was primarily from chalcocite, the infrared response was poor compared to that of the device heated for 2 minutes. Based on these observations, the heating period for the first stage of the fabrication of a device was chosen to be 2 minutes. The spectral response curves have not been corrected for the variation in intensity with wavelength of the exciting light which is shown separately in the figure. It was found that the uncorrected response curves could be correlated more easily with the RHEED observations, and indeed the correction has no effect on the interpretation[21]. The large values of the correction factor at short wavelengths tend to distort the corrected curves to such an extent that the spectral features are not so obvious as with uncorrected curves.

The spectral responses of the OCV shown in Figure 5.8 correspond to three devices prepared by depositing films of CuCl of the same thickness, 0.2 μm, on to substrates held at the same temperature of 35°C, but at three different rates of deposition of 200, 400 and 1000 Å per minute. The curves have been normalised to a common maximum value. The device produced at 400 Å per minute had the highest efficiency and contained the largest proportions of chalcocite. This is revealed by the broad peak at 0.96 μm in the spectral response. The phase was also checked by RHEED. In the device where the evaporation rate was very high, 1000 Å/min, the response at 0.96 μm was smaller, and a peak characterised by a slow response to changing wavelength appeared in the vicinity of 0.68 μm, indicating a response from copper levels in the CdS[18]. However with the device formed using the low deposition rate of 200 Å/mm, the response in the vicinity of 0.78 μm indicates the presence of djurleite.

When the thickness of the deposited layer was systematically varied, while the deposition rate and substrate temperature were kept constant, the resulting devices yielded the curves shown in Figure 5.9. These reveal that

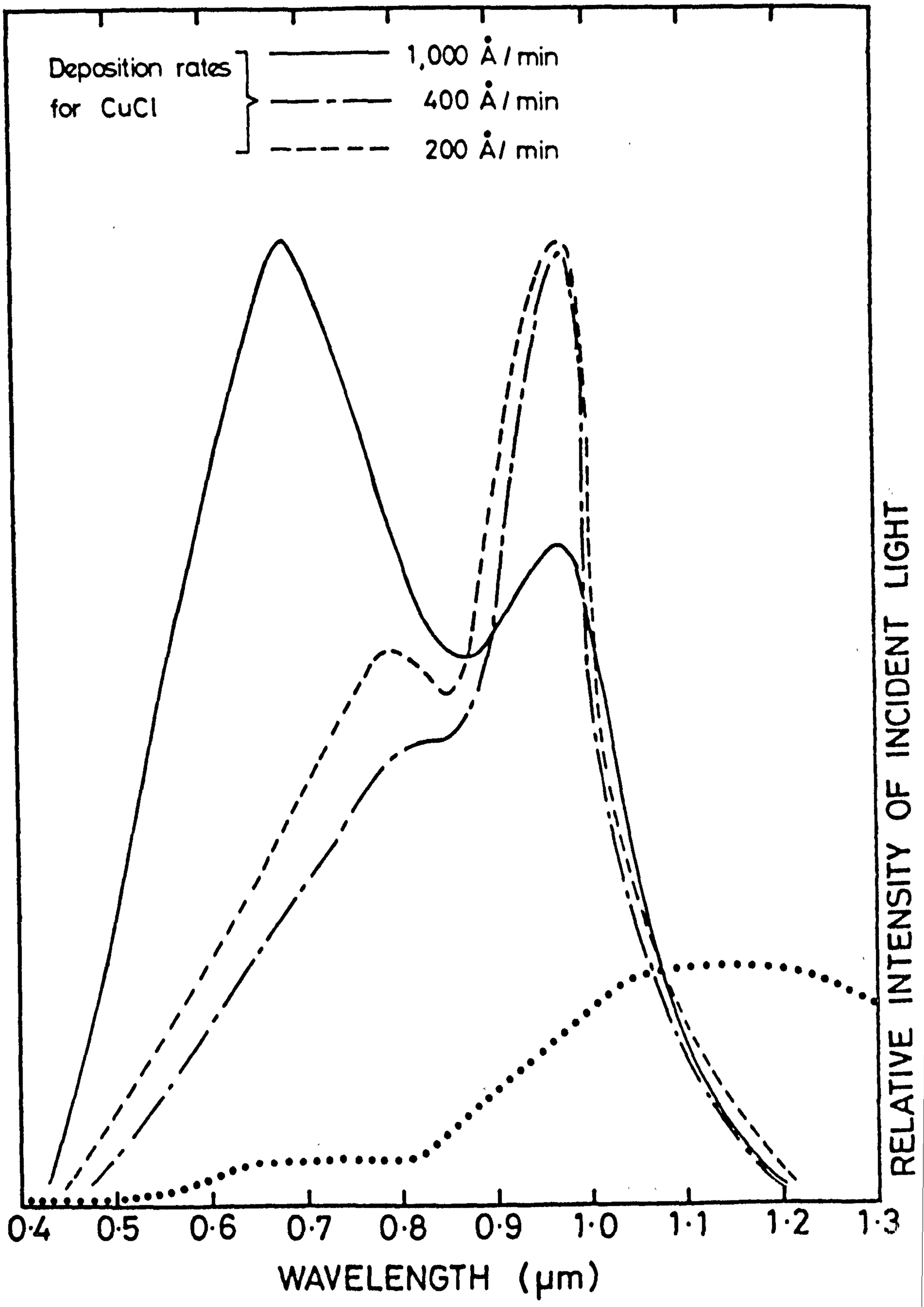


FIGURE 5.8: The dependence of spectral response on CuCl deposition rate.

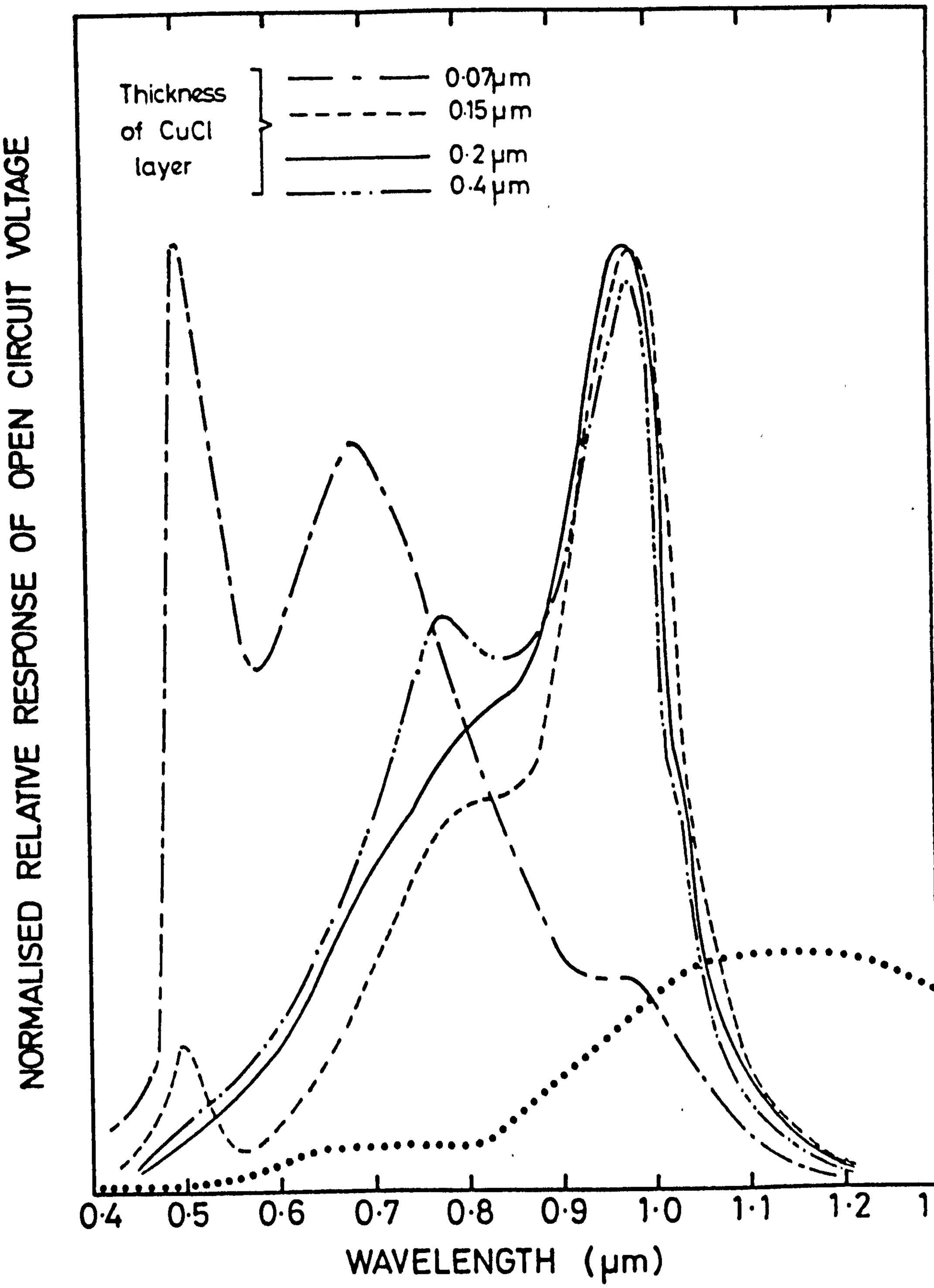


FIGURE 5.9: Spectral responses of heterojunctions formed with different thicknesses of CuCl.

the devices prepared with a CuCl layer 0.15 μm thick exhibited the largest relative response at 0.96 μm. However, this particular thickness of Cu_xS is sufficiently thin to allow the response from the band gap of CdS at about 0.5 μm to be detected. For the device prepared using a 0.2 μm thick layer of CuCl, the chalcocite peak was predominant, and a small shoulder due to djurleite appeared at 0.78 μm. However by increasing the CuCl thickness to 0.4 μm the proportion of djurleite was increased such that a definite but small peak appeared at 0.7 μm. It was also found that depositing an even thicker layer posed a problem in washing off the $CdCl_2$ and unreacted CuCl. At the other extreme, with very thin layers of CuCl (0.07 μm), the response was mainly due to djurleite and the band gap of CdS.

The effect of the substrate temperature during deposition on the phase of Cu_xS is revealed by the spectral responses shown in figure 5.10. Inspection of these curves shows that the maximum chalcocite response was obtained from the device for which the substrate temperature was held at 35^oC during the deposition. In the device fabricated at substrate temperature of 50^oC the peak at 0.7 μm had shifted to 0.62 μm. The RHEED pattern indicated the dominance of chalcocite at this stage. For the deposition performed with a substrate temperature of 90^oC, the resulting device had a dominant response corresponding to the band gap of CdS indicating a very thin layer of Cu_xS.

It is quite obvious from the RHEED study and the measurements of spectral response that the preparational parameters strongly affect the formation of Cu_xS layers on CdS. It was noticeable that an observation of chalcocite in the RHEED pattern corresponded with the appearance of a strong peak in the spectral response at 0.96 μm. However, it was always accompanied by a shoulder near 0.78 μm which indicated the presence of djurleite[19]. It is quite likely that the top surface is chalcocite which is detected by RHEED, while the phase at the interface is copper deficient. In fact a small amount of djurleite was invariably found in devices formed by the dry barrier process[9].

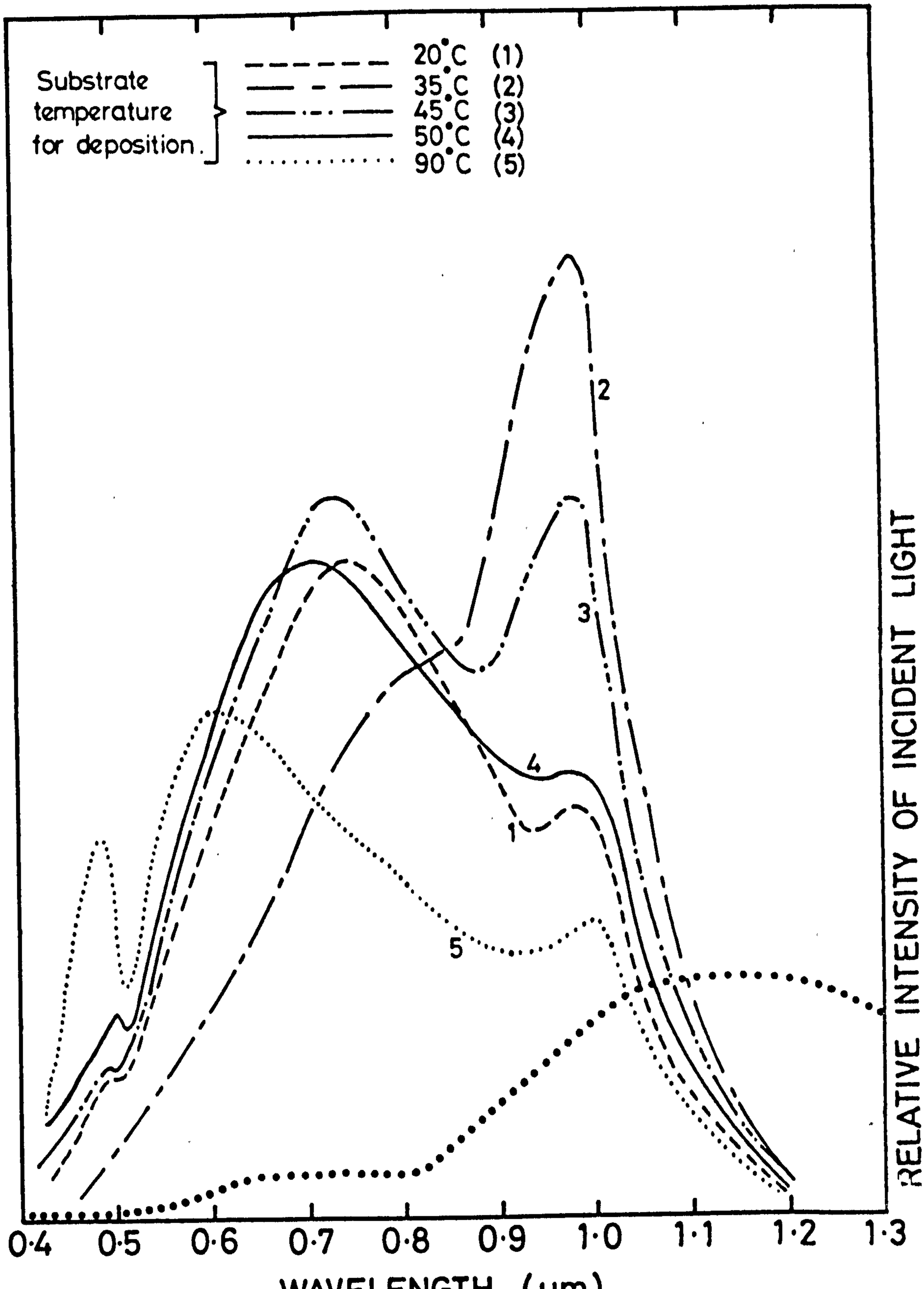


FIGURE 5.10: The dependence of spectral response on substrate temperature used during the deposition of CuCl.

The devices which RHEED showed carried a layer of djurleite gave a dominant peak near 0.7 μm in the spectral response[19]. Since djurleite has a poor absorption coefficient[22], the response at the band edge of CdS at 0.5 μm also increased.

In the devices where a mixture of chalcocite and djurleite was revealed by RHEED, broad peaks at 0.96 μm and 0.7 μm were observed in the spectral response. In the devices which were formed while keeping the substrate temperature $\gtrsim$ 50°C, the spectral response showed a shift towards shorter wavelengths (0.62 μm). There the response to changing wavelength became slow. This type of feature has been attributed by Caswell et al[18] to excitation from copper centres formed by diffusion of Cu into the depletion region of the CdS. In the present work this feature was observed in the following circumstances.

(i) with a high evaporation rate of CuCl

(ii) with high substrate temperatures ($\gtrsim$ 50°C)

(iii) after extended heat treatment

In devices prepared using these extremes the main response occurred at shorter wavelength and the peak lay between 0.7 μm and 0.6 μm. Following Caswell et al[18] it can be inferred that some copper diffuses into the depletion region in CdS making a compensated i layer which causes the response to resemble that of photoconducting Cu doped CdS. When the evaporation rate is very high, more copper diffuses into the CdS from CuCl, and this is reflected in a large cross over effect in the forward dark and light J-V characteristics. The same effect occurs in the device formed with substrate temperatures $\gtrsim$ 50°C.

The formation of the djurleite phase on the device prepared using a slow deposition rate (200 Å/min) can be attributed to the presence of the hexamer species which may exist in the equilibrium vapour phase near the melting point[23] and affect the phase of Cu_xS. In general trimeric and tetrameric species of CuCl are assumed to exist during the evaporation from the melt, and at this high temperature of 430°C, the hexamer species no longer remains in

the vapour phase[24,25]. Although the thermodynamics of the process have not been studied in detail, it has been found that the thermodynamical parameters affect the stoichiometry of the Cu_xS produced by the solid state reaction. These parameters and their effect on the evaporation of CuCl have been discussed by Brestovansky et al[26]. Their relevance becomes more obvious when comparing the stoichiometry of the sample prepared using substrate temperatures of 20°C and 35°C where the lower temperature leads to formation of some djurleite.

The thickness of the deposited CuCl layer also affects the Cu_xS formation. More djurleite is formed in layers 0.07 μm thick. This may be attributed to the loss of Cu from the chalcocite at the interface which leads to the formation of copper deficient phase near the junction[12]. When the layer of Cu_xS is thin, the response from the layer near the interface dominates indicating more djurleite. A small peak near 0.78 μm appeared in the response of a device when a 0.4 μm thick layer of CuCl was deposited, which may again be attributed to the presence of djurleite. On increasing the thickness of the CuCl further the red response decreased and the band near 0.7 μm increased suggesting a larger proportion of djurleite. It seems that the $CdCl_2$ by-product inhibits the reaction after some time[5], and the excess chlorine may cause a Cu deficient phase[8]. This sets a limit on the thickness of the chalcocite layer which can be produced by the dry barrier process[27].

The observations discussed above lead to the conclusion that the optimum chalcocite layer for photovoltaic purposes can be obtained by evaporating a layer of CuCl about 0.2 μm thick at an evaporation rate 400 Å/min on to a CdS substrate kept at 35°C, and subsequently administering a 2 minute heat treatment in argon at 200°C to promote the solid state reaction between the CdS and CuCl.

5.3.2 Temperature Dependence of Spectral Response

To examine the various Cu_xS phases formed on CdS in more detail the spectral responses were measured at 85K as well as at 295K. The different

phases of Cu_xS were produced deliberately by varying the preparational parameters appropriately and were identified by RHEED. In order to avoid the slow response associated with the copper levels, a few devices were fabricated by the wet plating technique which does not require heat treatment to form the heterojunction.

The curves in Figure 5.11 show the spectral response at 295K and 85K of two devices, one carrying a predominantly chalcocite and the other a mainly djurleite layer of Cu_xS. The chalcocite phase was obtained by evaporating an 0.15 μm CuCl layer on to the CdS which was held at 35°C. The evaporation rate was 400 Å/min and the sample was heated for 2 minutes. The second specimen was prepared by the wet plating technique using a plating temperature of 50°C since this leads to the formation of djurleite[18]. For each device the overall shape of the response at the two temperatures remained the same. The device with the chalcocite had a peak at 0.96 μm at room temperature and a shoulder at about 0.8 μm. The signal increased by a factor of 2 in the range of 0.7 to 1 μm when the temperature was reduced to 85K. A similar increase was observed in the same region of the spectrum for the device carrying the layer of djurleite when the temperature was reduced. However, no change in the response was observed in the range 1 to 1.2 μm. The small shift in the peak at 0.5 μm is due to the change in the band gap of CdS with temperature.

Figure 5.12 shows the spectral response of another two devices where one carried a layer which was mostly djurleite, while the other was fabricated so that it had a considerable response from the copper levels in the CdS. The djurleite layer was produced by depositing a 0.07 μm thick layer of CuCl on a CdS substrate at 20°C with an evaporation rate of 200 Å/min. The other device was formed by evaporating a 0.15 μm thick layer of CuCl at 400 Å/mm on to CdS at 50°C. At 295K both devices had a low profile at 0.96 μm and a pronounced shorter wavelength peak at 0.78 μm for the djurleite layer and 0.68 μm from the copper levels. At 85K the response became larger in the band

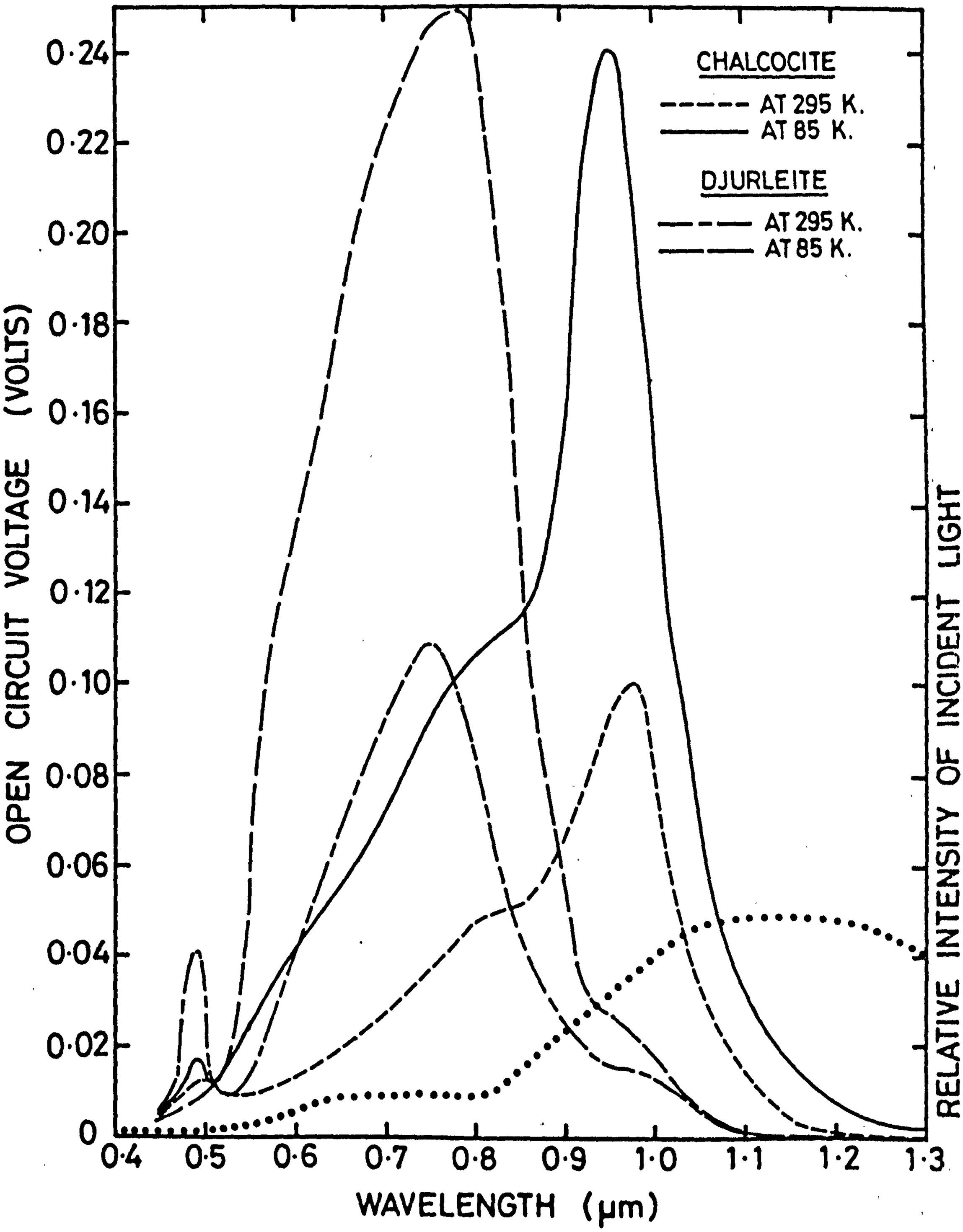


FIGURE 5.11: The effect of temperature on the spectral responses of the devices prepared separately with layers of chalcocite and djurleite.

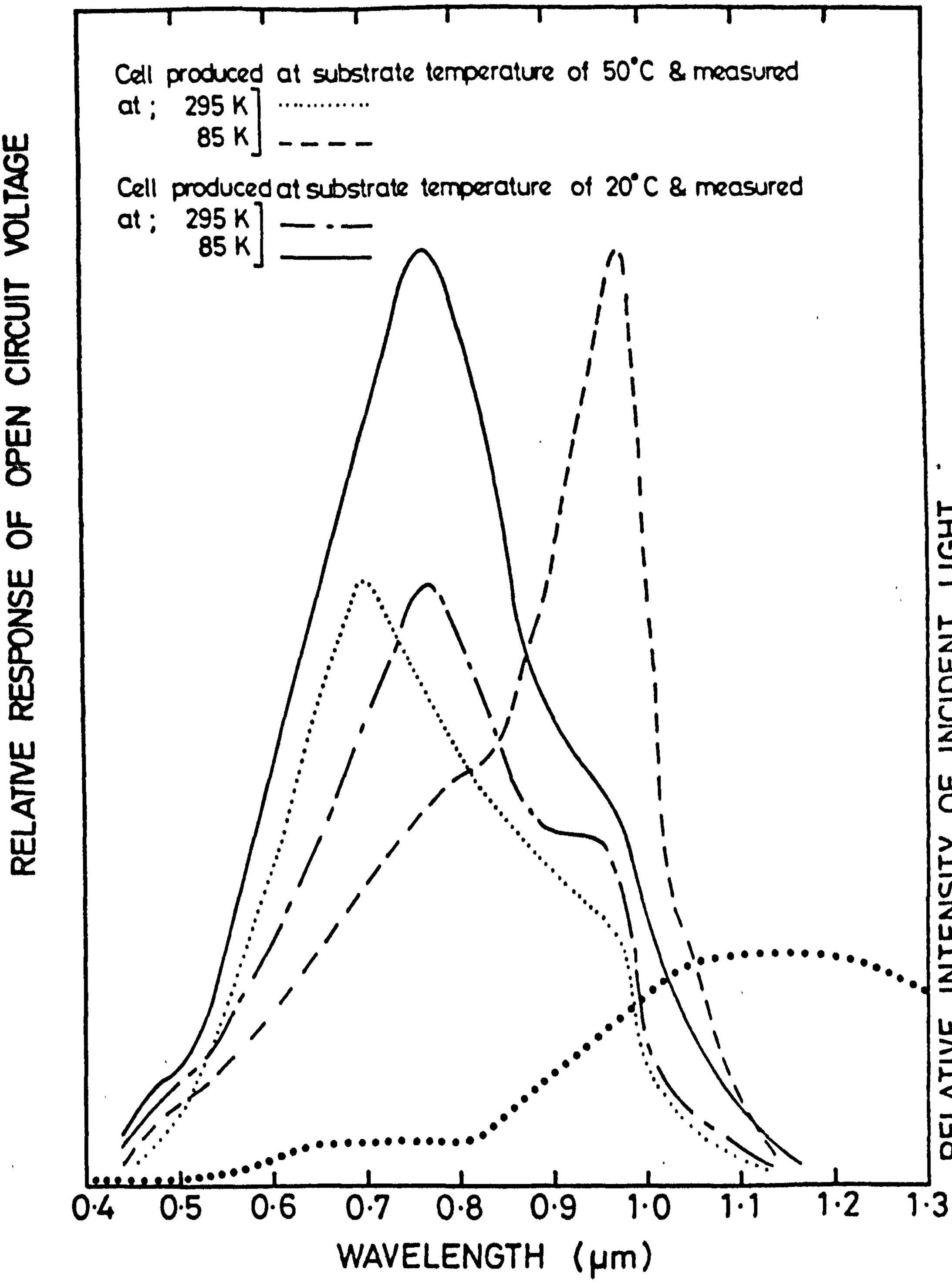


FIGURE 5.12: The effect of temperature on the spectral responses of

(i) A device prepared with a chalcocite layer and with copper levels diffused into CdS.
(ii) A device prepared with a djurleite layer.

of 0.7 μm for the device containing djurleite, while for the other cell the response at 0.6-0.7 μm diminished and a pronounced peak at 0.96 μm appeared which of course corresponds to chalcocite.

Since the responses due to djurleite and the copper levels lie in the same spectral region, a third type of device was fabricated which had both a djurleite layer and diffused - in Cu levels. The object of this was to observe the effect of reducing the temperature on the two responses in the same device. Such a device was prepared by evaporating a 0.2 μm layer of CuCl at 200 Å/min on to CdS held at 90°C. A large cross over effect was obtained between the dark and light J-V characteristics in forward bias. The spectral responses measured at 85K and 295K are shown in Figure 5.13. At room temperature the peak near 0.96 μm was small and a broad peak appeared near 0.68 μm. The response at 0.5 μm was quite large. At 85K, the response at 0.96 μm increased only slightly, but near 0.7 μm there was a two-fold increase compared with room temperature. In addition to this there was a pronounced shift of the peak from 0.68 μm to 0.78 μm.

A fourth type of device was then prepared to produce a mixture of chalcocite and djurleite without forming an i layer. The object of this was to avoid the response due to the copper levels, and to compare the relative responses of chalcocite and djurleite at 85 and 295K. This sample was fabricated by the wet plating technique. The temperature of the plating bath was kept at 80°C with the intention of producing a mixture of chalcocite and djurleite. RHEED observations indicated a mixture of the two phases, but with djurleite in predominance. The spectral response at 295K also evidenced the mixture of the two phases from the comparable magnitudes of the two characteristic peaks at 0.96 μm and 0.78 μm. When the temperature was reduced to 85K, the band at 0.7 μm (djurleite) was more pronounced than that at 0.95 μm(Fig.5.14).

In the dry barrier process, heating is an essential requisite for the formation of the device. The process results in the diffusion of some copper into CdS which produces deep acceptors[29,30], with hole ground and excited

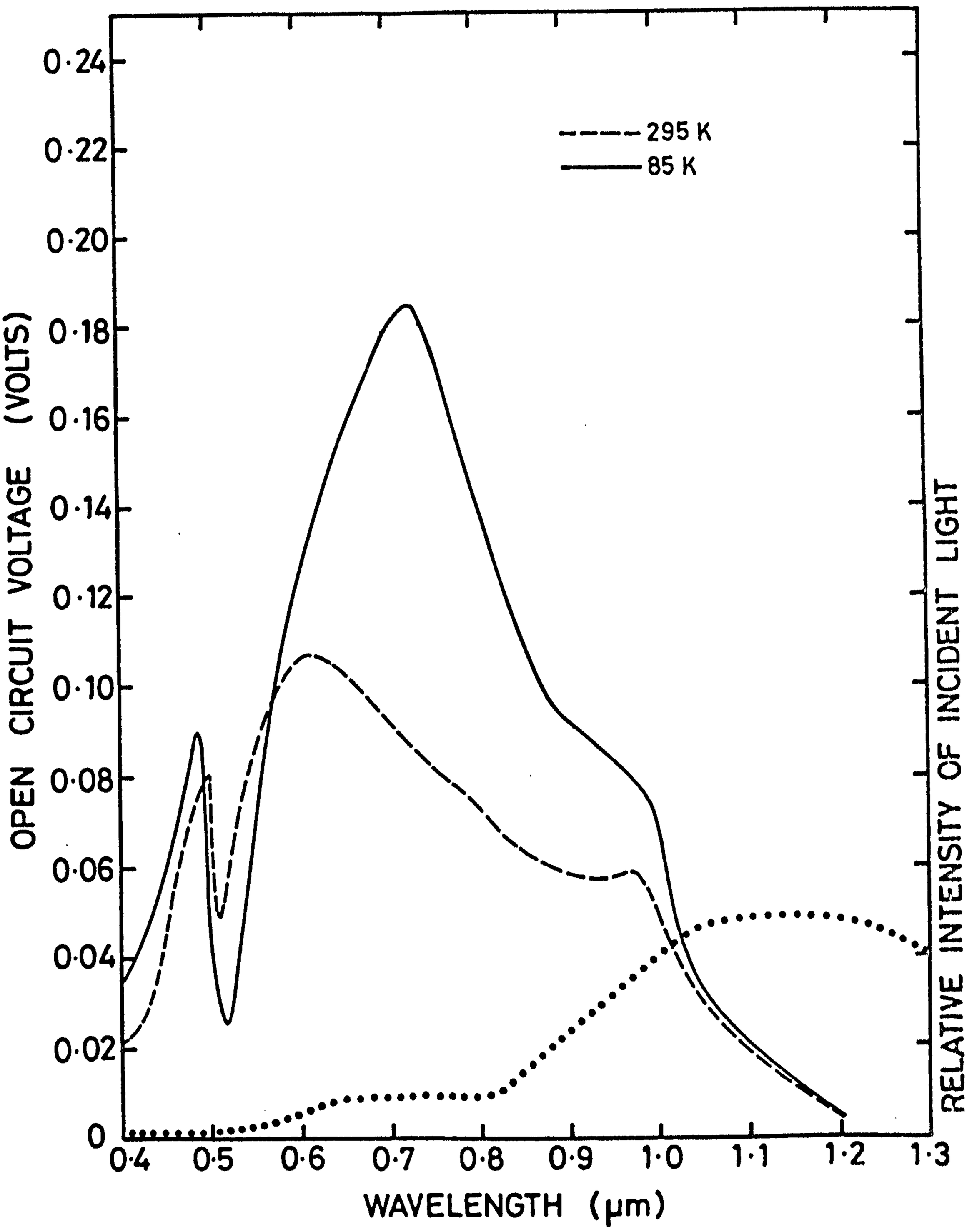


FIGURE 5.13: The effect of temperature on the spectral response of a device prepared with a djurleite layer and with Cu levels diffused into CdS.

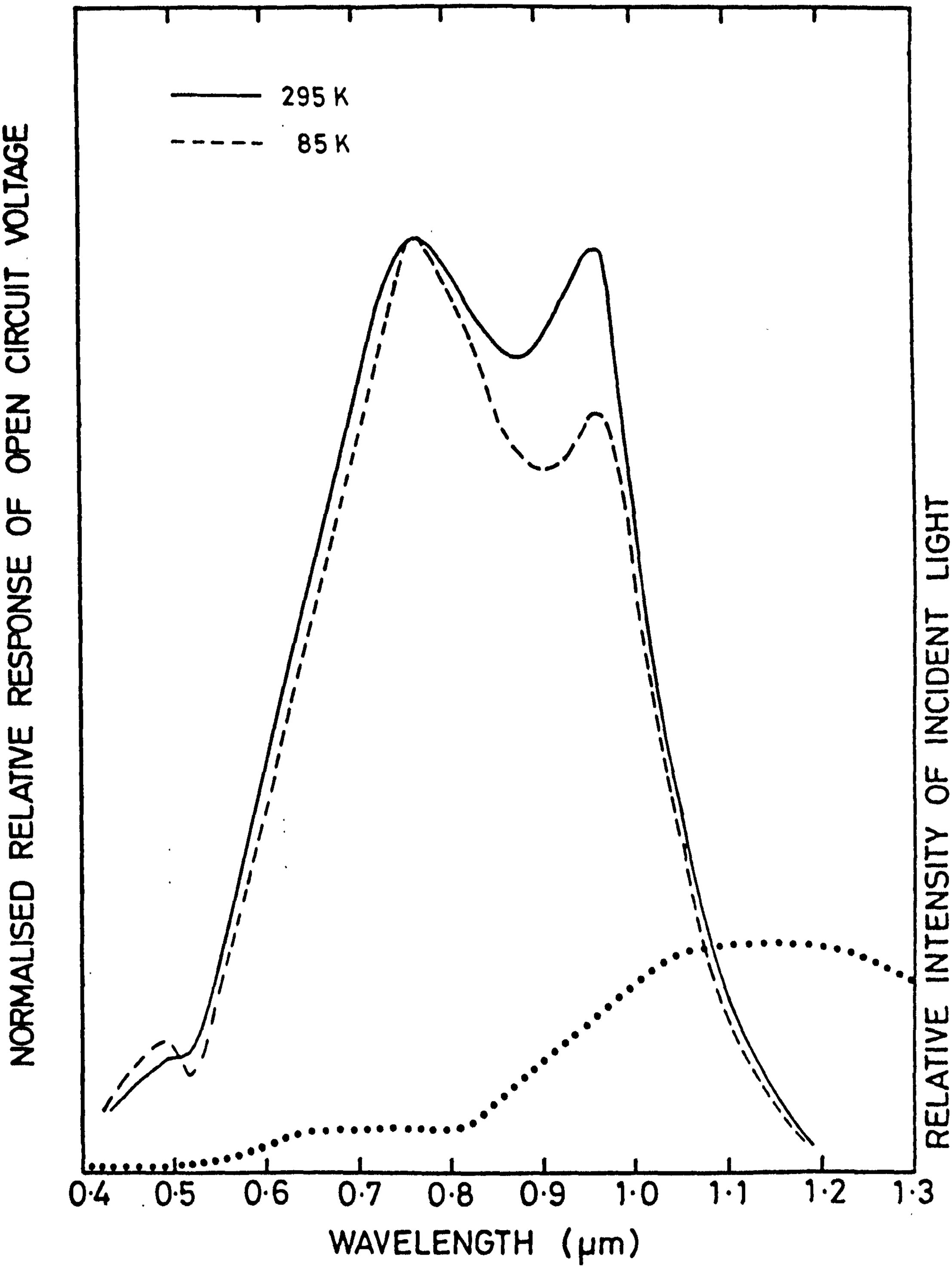


FIGURE 5.14: The effect of temperature on the spectral response of a device prepared with a Cu_xS layer comprised of a mixture of chalcocite and djurleite.

states 1.1 and 0.35 eV above the valence band[31]. The spectral response of the device would therefore be a super-position of the response of the Cu_xS layer and that of the copper levels in CdS which depends on the preparational parameters[32,33]. A broad response between 0.6 μm - 0.7 μm has been attributed to the copper levels which are characterised by a slow speed of the response to a change in wavelength or intensity. This response could be the result of the excitation of electrons to the conduction band by a green light from deep levels 0.35 eV above the valence band. These electrons are swept away by the field of the depletion region and at the same time the holes are thermally freed to the valence band and move towards the interface. The work described here shows that the response associated with the copper centres diminishes at 85K which can be attributed to the elimination of the process of the thermal freeing of holes at low temperature.

In general the OCV at 85K is much larger than at 295K. This can be attributed to the lowering of the reverse saturation current with reduction in temperature, which effectively enhances the OCV. Wysocki and Rappaport[34] suggested that the effect of temperature on the device parameters was primarily due to the change in the intrinsic carrier density.

Our study reveals that the region in the spectrum where the effect of the lowered temperature is most pronounced depends upon the phase of Cu_xS present in the devices. Hence the increase is in the band at 0.9 μm for devices with chalcocite layers, but is at 0.7 μm when the phase is djurleite(Figs 5.11-5.13). Furthermore, when a mixture of chalcocite and djurleite was obtained by the wet process in which the probability of the response due to copper levels was minimised (Fig. 5.14) the relative enhancement at 85K of the response corresponding to djurleite was in agreement with the RHEED assessment of the composition of the Cu_xS layer. This indicates that the relative enhancement of the response peaks at 85K can be an accurate indication of the predominant phase of Cu_xS. This reasoning is confirmed by the device prepared on a

substrate at 50°C (Fig 5.12) where there was a sharp rise in the response at 0.96 μm at 85K, corresponding to the chalcocite phase. Similarly the shift in the peak of the response in Fig 5.13 from 0.68 μm to 0.78 μm and the enhancement of the signal in this region of the spectrum reveals the djurleite phase. These observations suggest that a better indication of actual phase of the Cu_xS layer is obtained by measuring the response at 85K.

5.3.3 Current Voltage Characteristics

The current voltage characteristics of different devices were measured under forward and reverse bias in the dark and under AM 1 illumination. The characteristics of the as-made devices varied from die to die from different boules. In particular as discussed earlier in the section 5.2.1, surfaces with two different types of topography were observed on the $(00\bar{1})$ CdS plane after polishing and etching the dice. The J-V characteristics of the as-made devices were affected by these different topographies. Typical examples of good J-V characteristics measured in the dark and under AM 1 illumination as shown in Fig 5.15. This type of heterojunction was fabricated under the optimum conditions, i.e. with a 0.2 μm thick CuCl layer deposited on to a substrate at 35°C at a rate of 400 Å per minute, followed by heating in argon at 200°C for 2 minutes. The reverse bias characteristic was quite hard, the fill factor was about 65%, the values of V_{oc} and J_{sc} were 0.54 volt and 18 mA/cm^2 This gave an overall efficiency of 6.3% under AM 1 illumination.

A few more dice were selected from the same CdS boule from which the device responsible for the characteristics in Fig.5.15 was prepared and these were etched in concentrated HCl for different periods of time. In the first instance the samples were etched for 5 seconds which enabled the Cd and S faces to be distinguished. After providing indium contacts on to the Cd faces, separate dice were etched for periods of 5, 15, 20, 25, 35 sec., thus making the total etching period for each 10, 20, 25, 30 and 40 seconds. Subsequently heterojunctions were made on these substrates as described in the previous

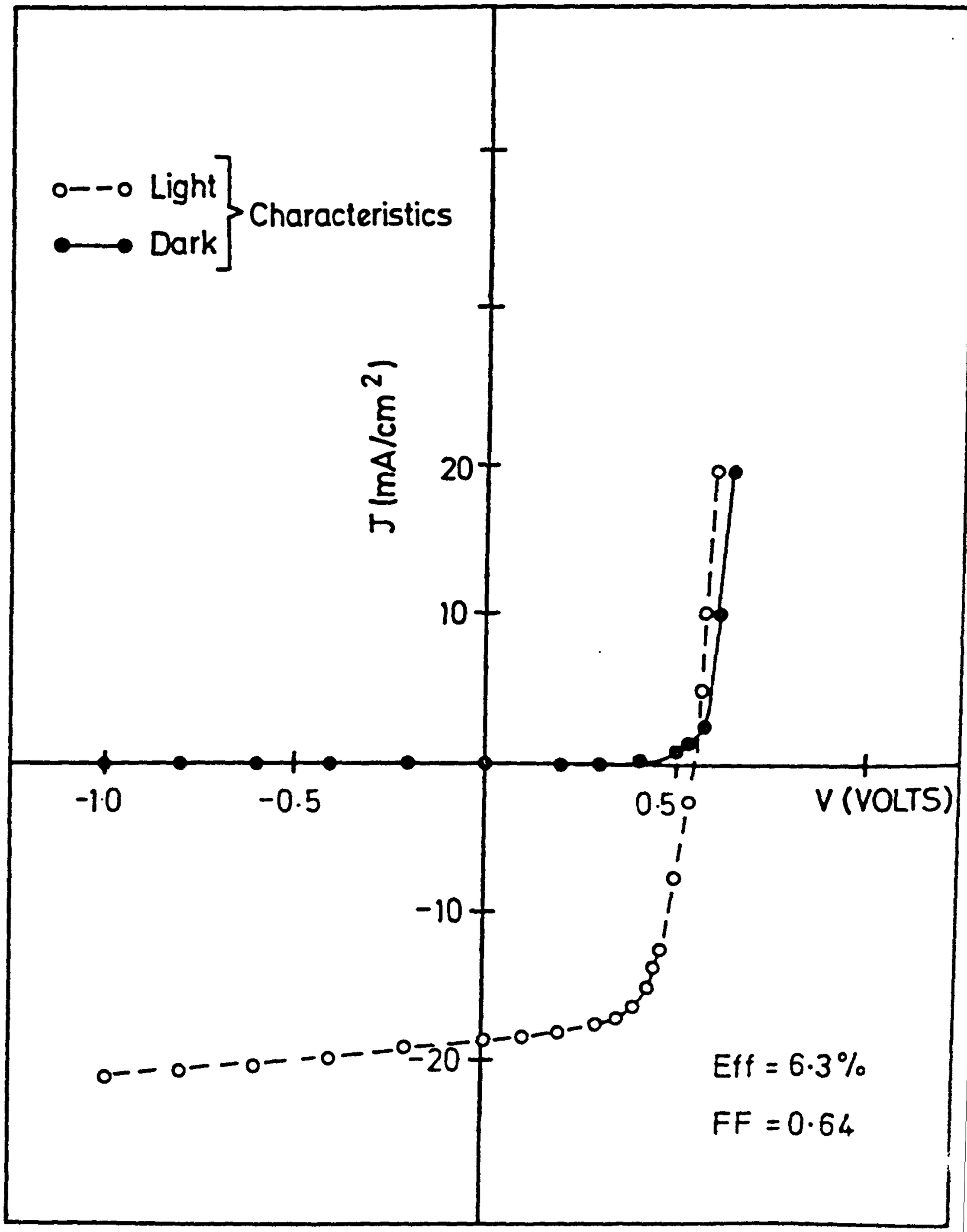


FIGURE 5.15: Current-voltage characteristics of a typical cell prepared under optimum conditions.

section. The J-V characteristics in the as-made conditions of these devices measured in the dark and under AM 1 conditions are shown in Figure 5.16. This figure does not include the J-V characteristics of the device etched for 30 secs which has already been shown in Figure 5.15. From these curves it is obvious that the devices etched for a total of 25 and 30 sec gave very hard reverse bias characteristics, good fill factors and high OCV s under as-made conditions, while those etched for total periods of 10, 20 or 40 sec gave soft characteristics with a poor OCV. The SCC obtained with the sample etched for 30 sec was the highest of all the devices. Heterojunctions were formed on the Cd faces also for comparison purposes and their J-V characteristics were always found to be inferior. A typical example of the J-V characteristics of a device on Cd face etched for 30 secs is also shown in Figure 5.16.

To account for the dependence of the characteristics on the etching period, it is necessary to consider the overall process of device fabrication. In the very first stage the crystal is cut into slices with the c-axis perpendicular to the large area surface. This produces deep saw marks on the crystal surface. To remove them the slices are mechanically polished using progressively smaller grit size of alumina powder ending up with 1 μm particles. Using the RHEED technique, Russell et al[1] found that the polished surface exhibited a sphalerite cubic structure. The sample is etched to remove this layer and also any other mechanical damage created by the polishing. The etching has frequently been found to affect the junction properties[4,35,36,37]. The optimum period of etching is expected to depend on the nature and thickness of the top polycrystalline layer. Removal of this layer is necessary in order to obtain a proper phase of Cu_xS, particularly when working with single crystal substrates. When the etching time was short (10 or 20 sec) the curves in Figure 5.16 revealed poor device characteristics corresponding possibly to a high density of surface states. As the etching period is increased, the top damaged layer is just removed leaving, it is suggested, a thin insulating layer

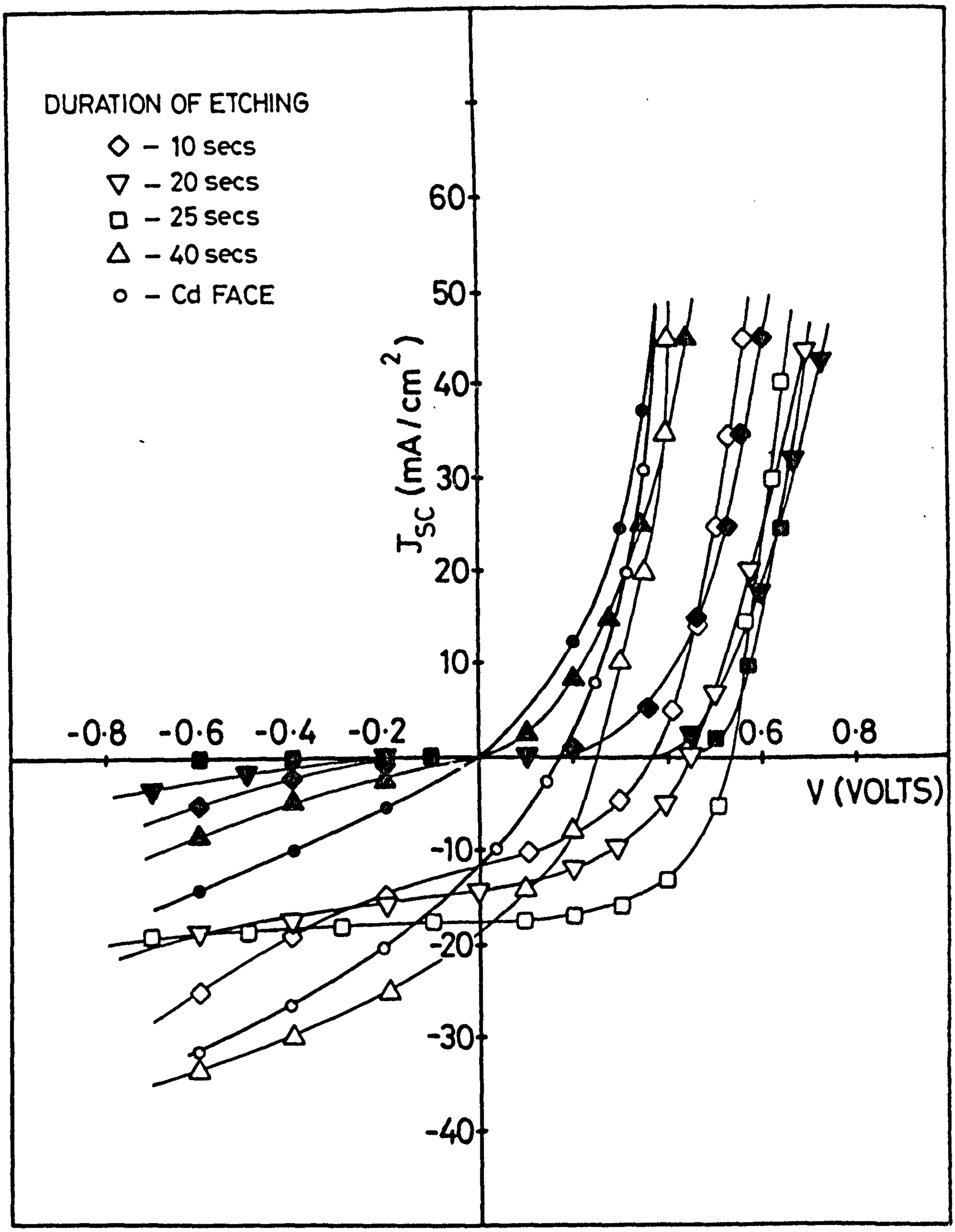


FIGURE 5.16: Current-voltage characteristics of devices formed on single crystal substrates after different periods of etching.

(Open symbols : light characteristics, filled symbols : dark characteristics)

which promotes a hard J-V characteristic. Etching for periods exceeding 30 secs causes more shunting paths, presumably due to high conducting regions on the surface around the junction and hence a softer characteristic is again obtained.

Although the best performance for a cell in the as-made conditions was obtained after etching for 30 secs, the J-V characteristics were not easily reproducible in a consistent way. The reason for this might be attributed to local variations in the properties of the CdS boule itself, or to some uncontrolled function of the polishing procedure leading to different thicknesses of the polycrystalline layer.

In most as-made devices the J-V characteristics measured under AM 1 illumination were found to be soft and the F.F. and S.C.C. were poor. Typical curves showing the J-V characteristics of four devices which had been heat treated for 1, 2, 5 and 10 minutes respectively are shown in Figure 5.17. In all these devices a 0.2 μm thick layer of CuCl was evaporated on the sulphur face of the CdS which had been etched for 30 seconds. The substrate temperature was kept at 35°C and the deposition rate was 400 Å/min. It is quite obvious that the reaction was completed after heating the sample for 2 minutes and further heat treatment led to a reduction in J_{sc}. In most devices giving soft J-V characteristics similar to those shown in Figure 5.17, the surface of the CdS was found to possess a high proportion of small rounded hillocks as described in section 5.2.1. The topography of the sample has previously been found to affect the J-V characteristics of devices prepared by the wet plating technique[38]. It seems that the topography can also influence the characteristics of devices formed using the dry barrier process. Since the etching time was also found to affect the J-V characteristics, the removal of the polycrystalline CdS layer in an optimal way may be a significant contributory factor in obtaining a good device.

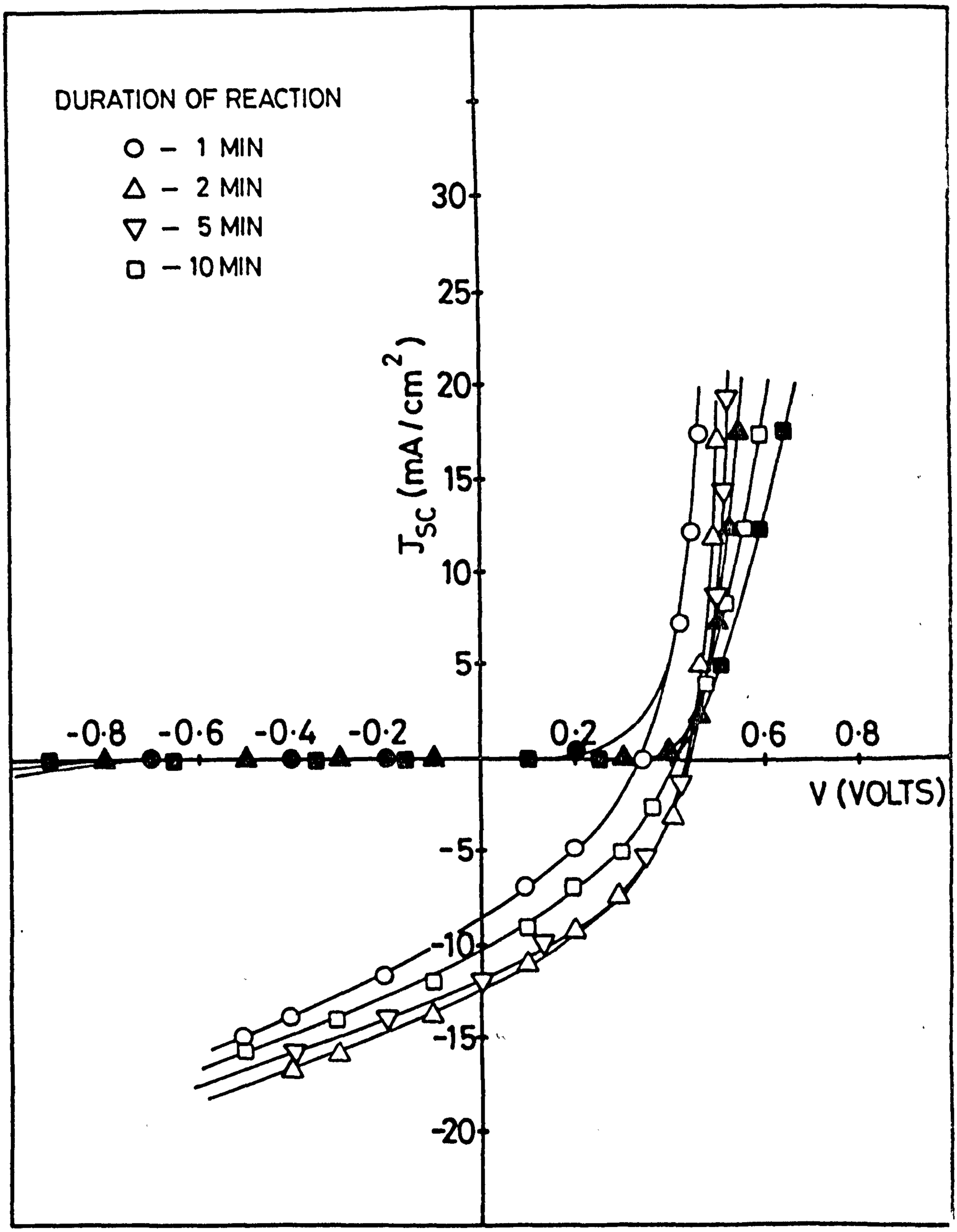


FIGURE 5.17: The effect of the duration of the reaction process on the current-voltage characteristics of as-prepared devices.

(Open symbols : light characteristics, filled symbols : dark characteristics)

5.4 PROPERTIES OF HETEROJUNCTION AFTER POST BARRIER HEAT TREATMENT

5.4.1 J-V Characteristics

To improve the performance of those devices where the characteristics were not good under as prepared conditions, post preparative heat treatments were administered. A typical example of the more usual J-V characteristic of an as-made device on dice with small hillocks (spongy surface) is shown in Figure 5.17. Though the OCV was reasonable (0.46V), the SCC was only 12.5 mA/cm^2 and the FF was 39.5%. To determine the optimum post barrier heat treatment, some cells were heated in air and others in argon for different periods of time. The J-V curves in Figure 5.18 and Figure 5.19 show the effects of heating devices in air and in argon at $200^{o}C$ for 7 and 10 minutes respectively. The heating in argon for 7 minutes produced a hard characteristic, with the OCV increased to 0.53V and a 25% improvement in SCC. The FF was also substantially increased to 64%. With devices heated in air for 7 minutes at $200^{o}C$ the OCV increased to 0.51V, the SCC also improved, but the fill factor was only 0.5, much lower than that following the comparable heating in argon. Under illumination, the J-V characteristics of the devices heated in air displayed kinks at forward and reverse biases of about 0.4V but no such kinks were observed in the characteristics of the devices heated in argon.

The effects on OCV, SCC, FF and η of different periods of post barrier heat treatment in air or in argon are compared graphically in Figure 5.20. Heating in air led to more immediate improvements in OCV, SCC and η which are apparent after 2 minutes. The maximum value of each of these parameters occurred after 4 minutes. In contrast, the improvements in the same parameters accompanying heat treatment in argon proceeded more slowly but continued for a longer time. Their maximum values were not reached until after about 7 minutes. Although the cells heated in air yielded slightly better values of SCC, their fill factors were inferior, particularly after 4 minutes which accounted for the poorer efficiency in air heated samples. Thus the most efficient cells were

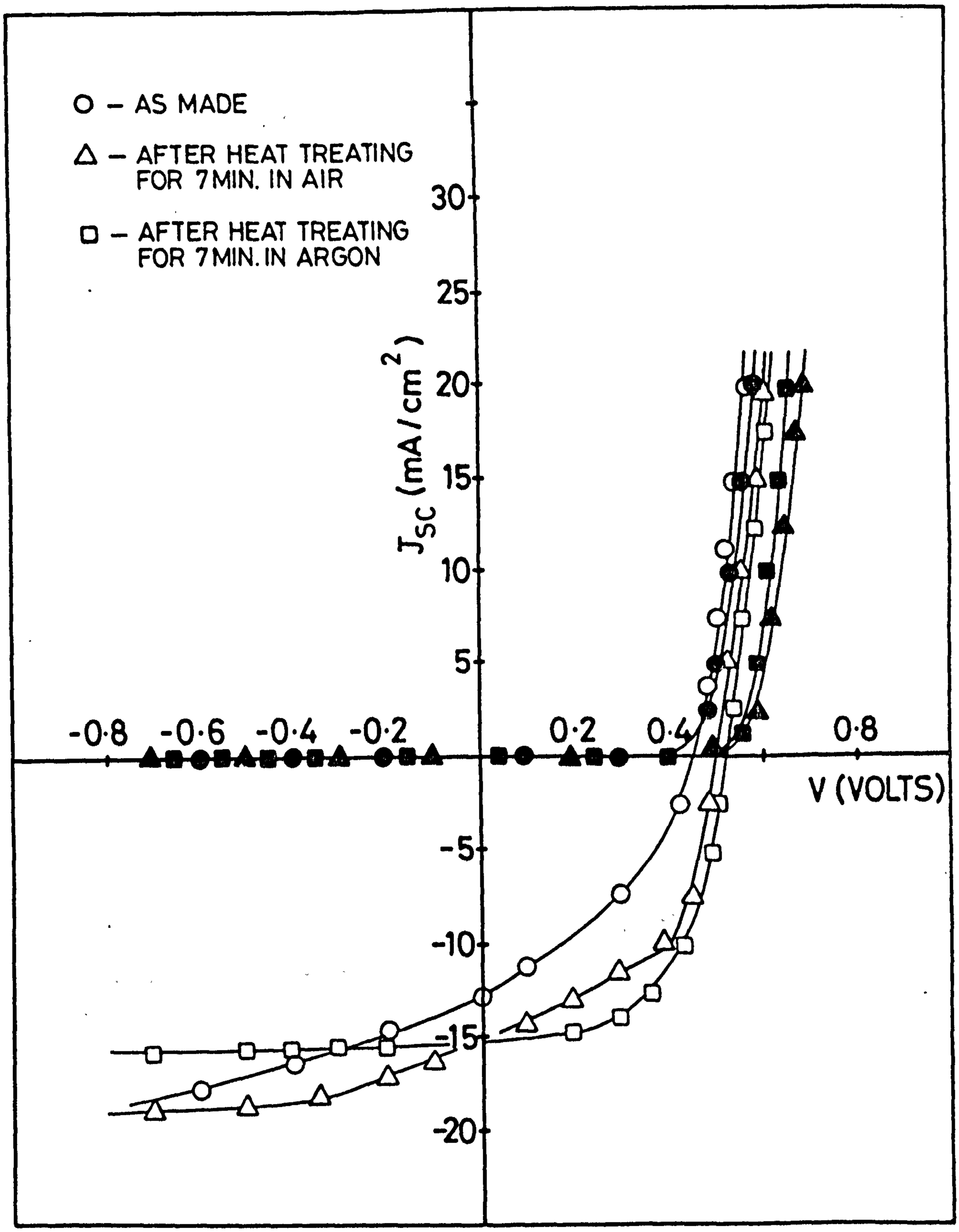


FIGURE 5.18: Current-voltage characteristics of devices after carrying out heat treatments separately in air and in argon at 200°C.

(Open symbols : light characteristics, filled symbols : dark characteristics).

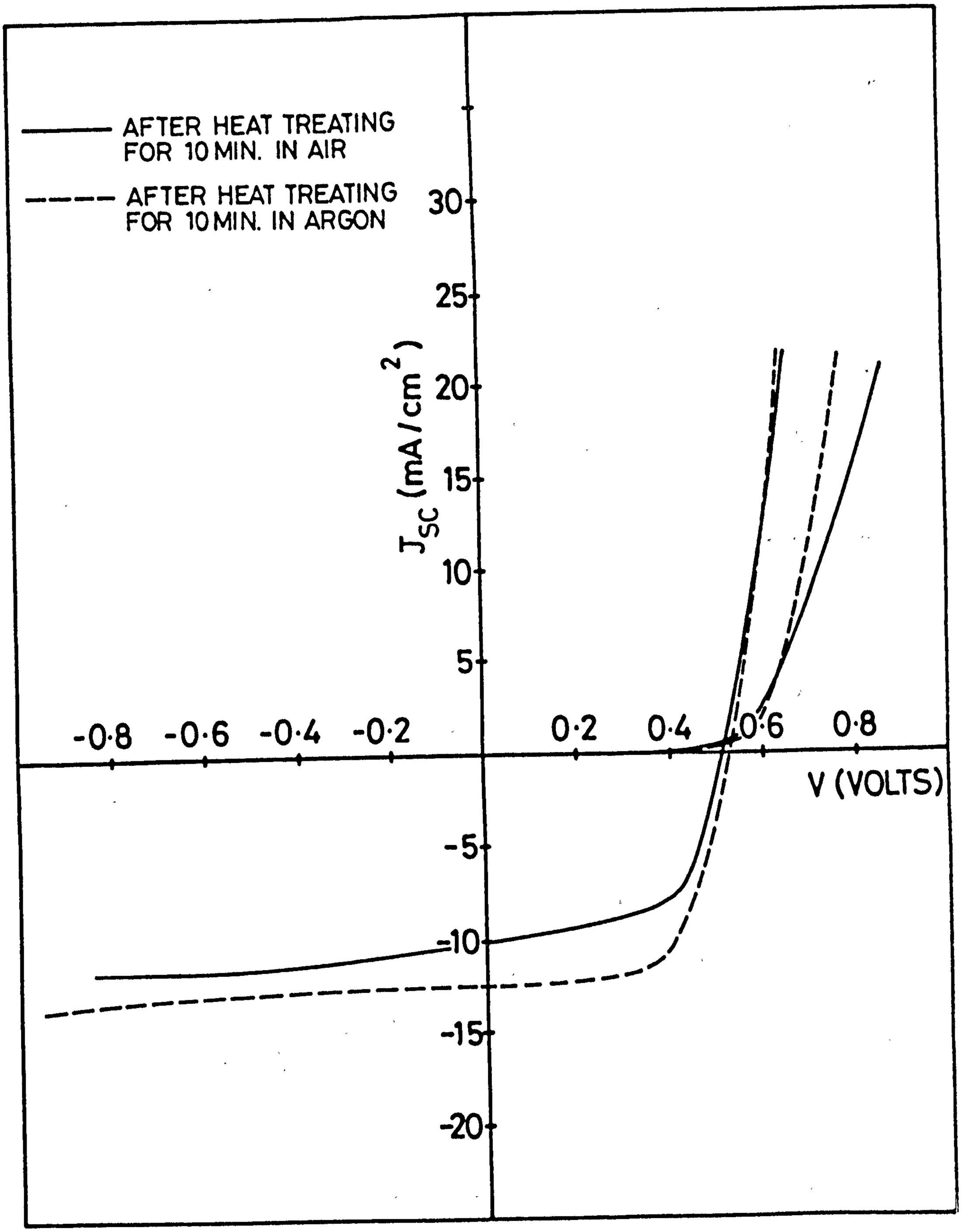


FIGURE 5.19: Current-voltage characteristics of devices heat treated at 200°C separately in air and in argon for 10 minutes.

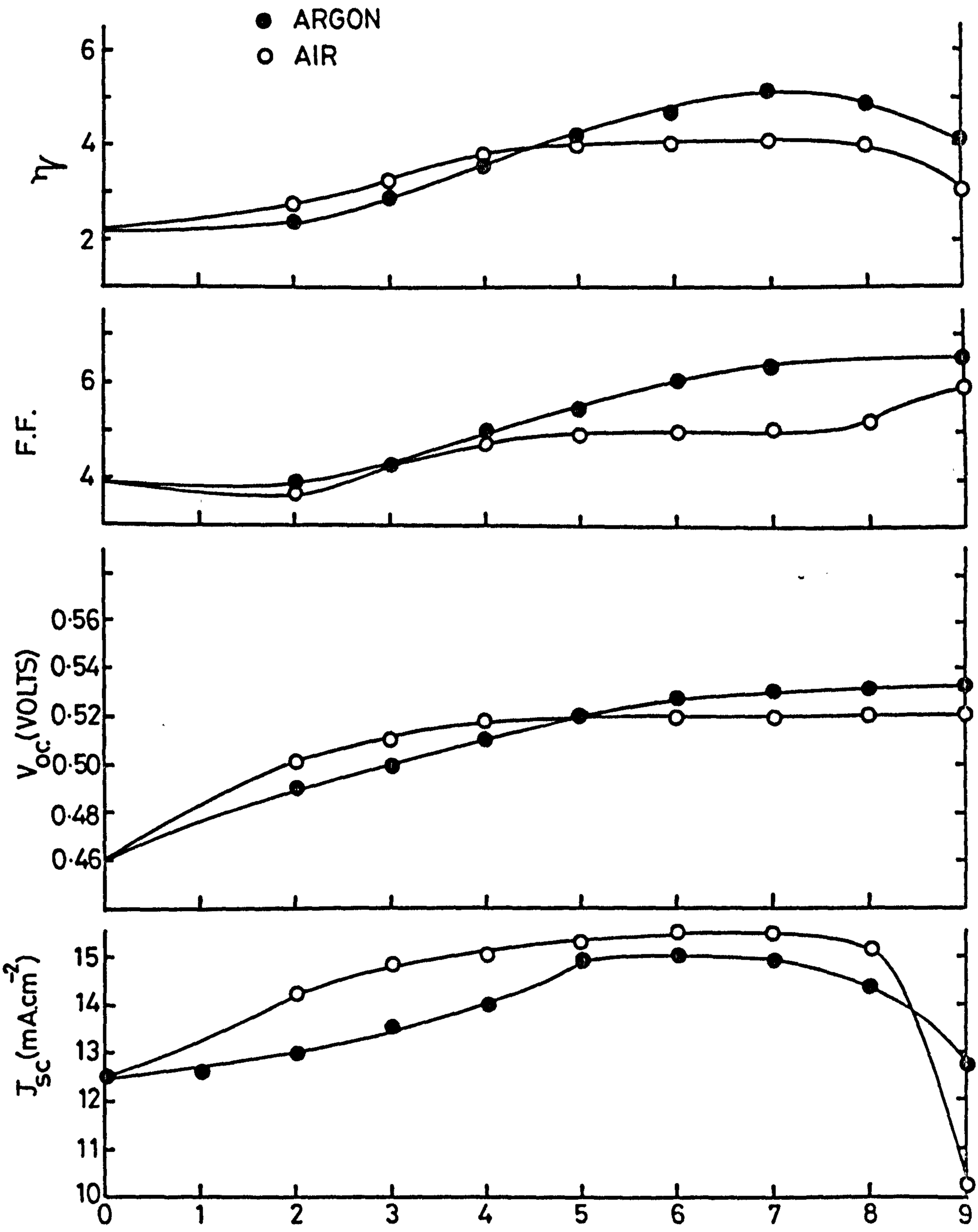


FIGURE 5.20: The effect on individual device parameters of the duration of heat treatments carried out separately in argon and in air at 200°C.

those heated in argon. A few samples heated in an H_2/N_2 mixture at 200°C for 7 minutes gave J-V characteristics similar to that obtained after heating in argon, though initially the device was softer. In general most of the devices were prescribed heat treatments in argon for 7 minutes to optimise their performance.

The effect of this optimised heat treatment was then studied on the devices which were prepared on dice etched for different lengths of time (Fig 5.21). The J-V characteristics of these devices have already been discussed in section 5.5. Poor as-made devices were improved by heat treatment, but good devices formed on surfaces etched for 25 and 30 seconds deteriorated. It has already been mentioned that as-prepared devices from a few selected boules gave good J-V characteristics if the deposition of the CuCl was preceded by a 30 second etch. The OCV of devices on lightly etched dice (10 seconds) was only 0.4V which suggests that numerous surface states were present at the interface affecting the device performance adversely. The SCC obtained from the device etched for 40 seconds was larger than that obtained from the most efficient device (those etched for 30 secs), but the OCV was considerably lower, 0.46V compared to 0.54V. The lower OCV may be associated with the large numbers of kink sites and ledges produced after lengthy etching. The slight increase in the SCC for these devices may be a result of a low series resistance, since the hard characteristic obtained after 25 and 30 sec etches is thought to be due to a very fine polycrystalline layer which affects the J-V characteristic but nonetheless provides more resistance. It is suggested that this is the reason why the sample etched for 30 seconds led to a larger SCC than the sample etched for 25 seconds, though both had hard characteristics. After heat treatment, all the devices had hard reverse bias characteristics, with fill factors of around 0.6. The device formed on the Cd face also showed improvement after heat treatment but only to the extent that the OCV reached a maximum value of 0.4 volt and SCC 10 mA/cm^2.

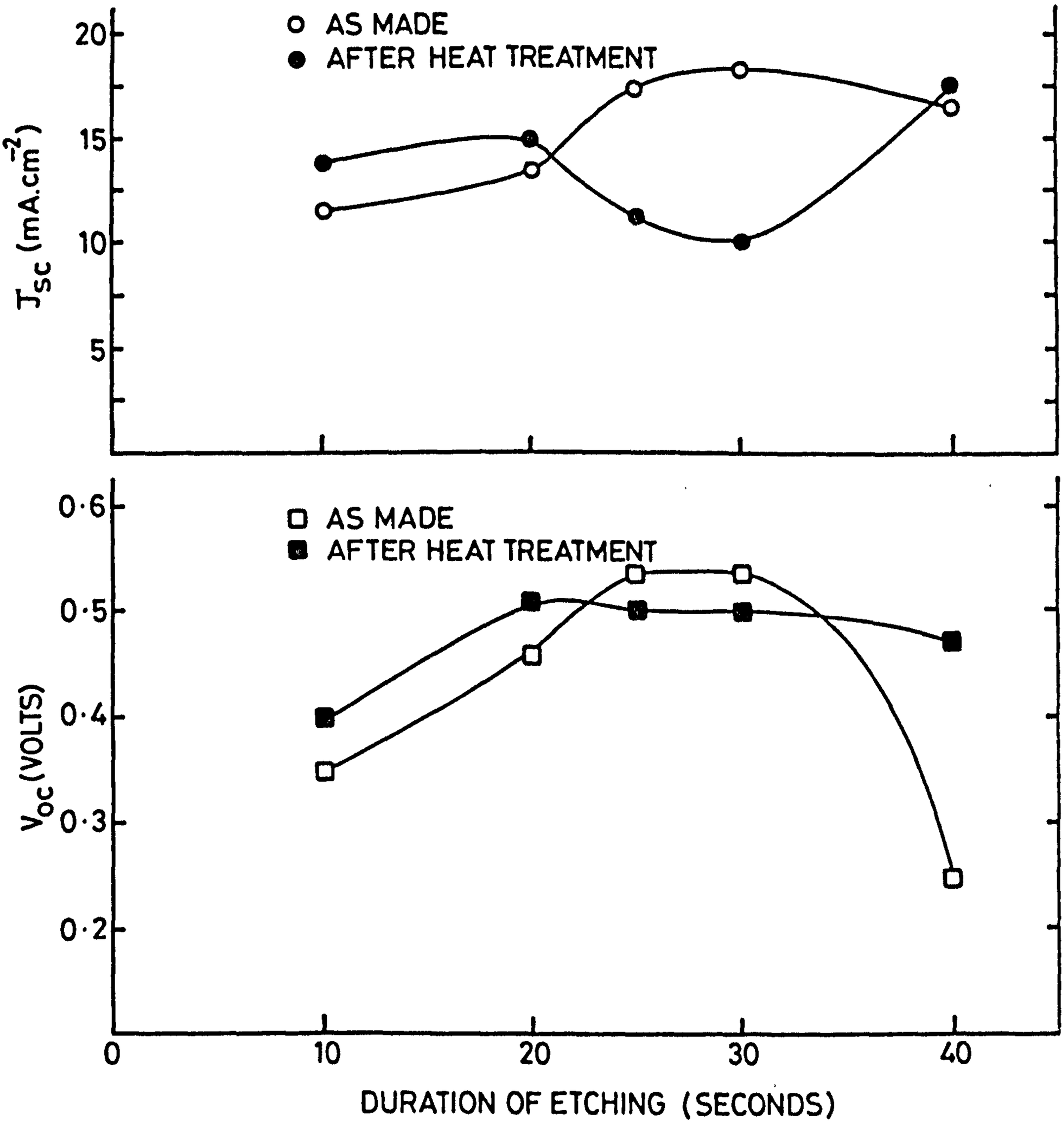


FIGURE 5.21: The effect of post barrier heat treatment on the characteristics of devices formed on CdS surfaces etched for different periods.

The devices prepared by depositing different thicknesses of CuCl and heating for 2 minutes in argon were subsequently heated in argon for 7 minutes to optimise their performance. The shape of the J-V characteristic of such an as-prepared device was similar to that shown in Figure 5.18. The performance of the devices made with different thicknesses of CuCl are summarised in Figure 5.22. It is obvious that the efficiency increased from 3 to 5% as the thickness of CuCl increased from 0.07 μm to 0.15 μm. It then saturated before decreasing as the thickness exceeded 0.3 μm. The decrease is attributed to the formation of a large proportion of djurleite (see section 5.3.2.).

5.4.2 Series Resistance

The series resistances of the various devices before and after heat treatment were measured using the flash lamp technique[39] described in section 4.9, Chapter 4. Accordingly, with an incident intensity of the light sufficient to saturate the total cell current measurements of the output voltage were made across different load resistors. Figure 5.23 shows the variation of the series resistance of the samples heated in air or in argon for different periods of time. After heating a device in air for 2 minutes the series resistance increased from 2 Ω to 2.4 Ω . After further heating, the series resistance decreased sharply to 1 Ω, and fell steadily to a value of 0.8 Ω after 6 minutes. Then the resistance increased again, reaching a maximum value of 3.1 Ω . In contrast, heat treatment in argon caused the series resistance to decrease slowly to a value of 1.2 Ω, and after 7 minutes it increased slowly to 1.75 Ω. The series resistances of the devices formed after etching the CdS from 20 and 40 secs respectively were also determined. These devices which were heat treated for 7 minutes in argon at 200°C and were found to have series resistances of 2.5 Ω and 0.9 Ω respectively.

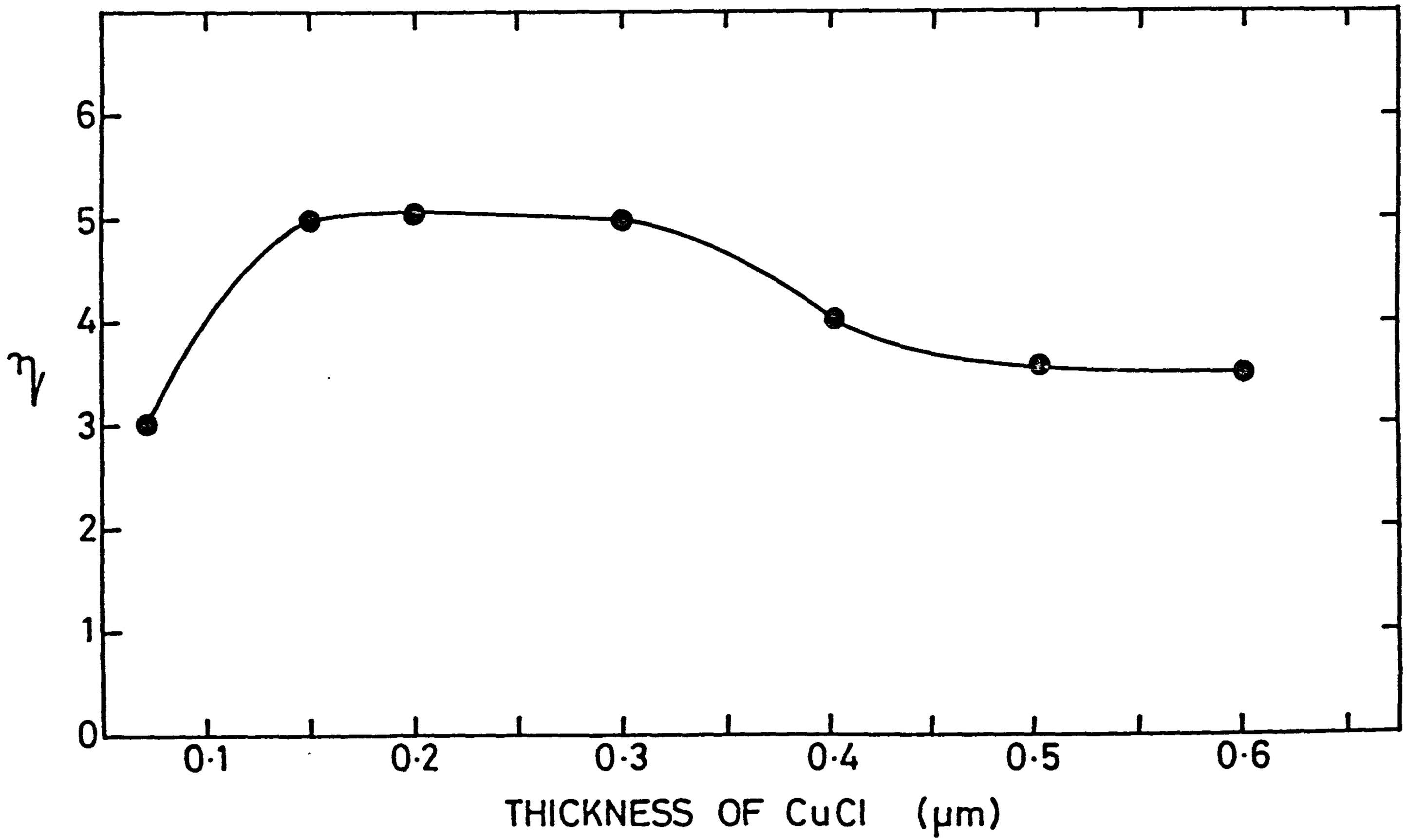


FIGURE 5.22: The effect of the thickness of the deposited CuCl layer on the efficiency of devices.

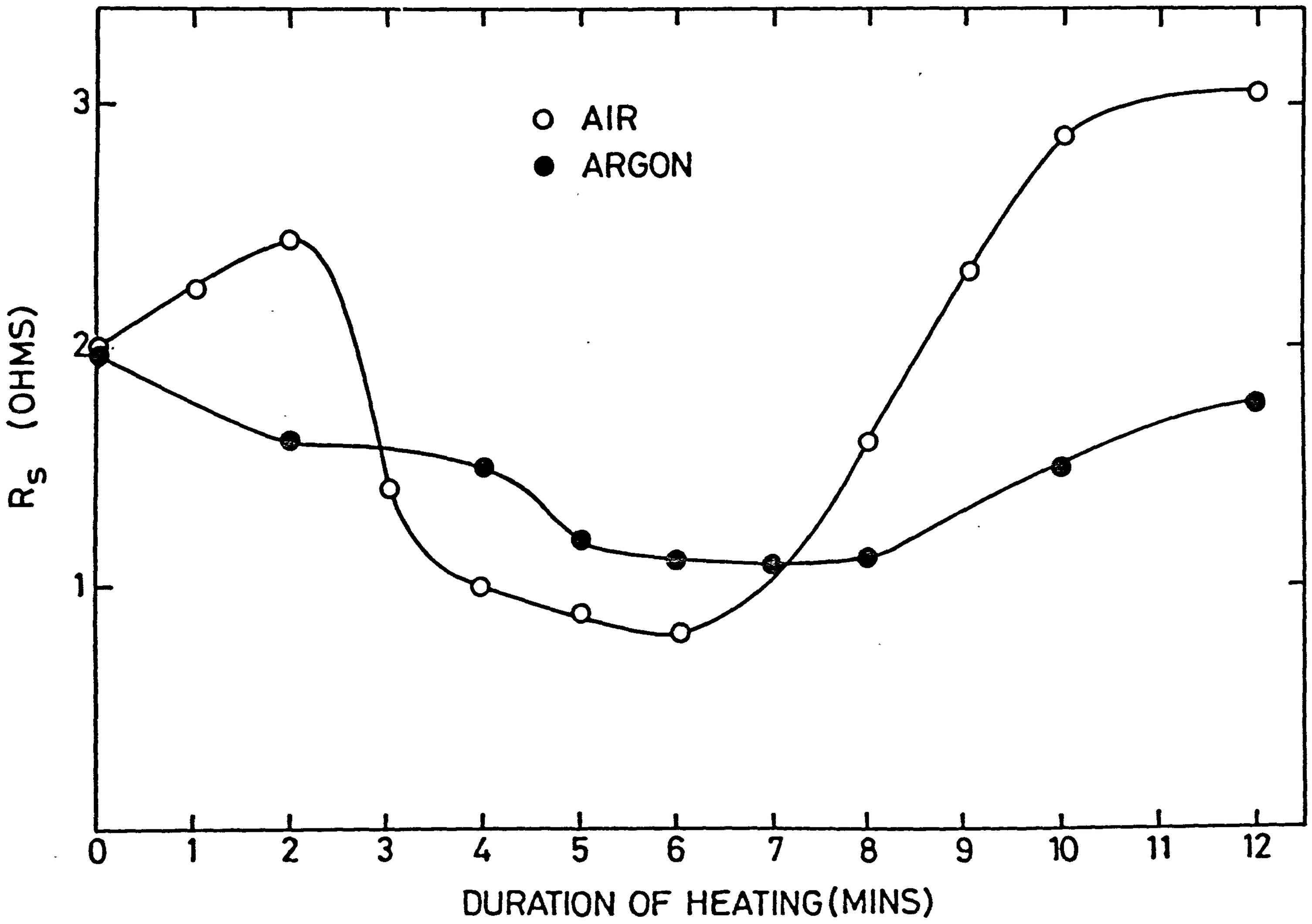


FIGURE 5.23: The variation of series resistance with different heat treatments.

5.4.3 Comparison with Wet Plated Devices

The properties of the dry barrier cells were compared with those of heterojunctions prepared by the wet plating technique[40]. The J-V characteristics of wet plated cells in the as-made condition and after heat treatment in argon for 7 minutes are shown in Figure 5.24. By comparing the curves of Figures 5.19 and 5.24, it is clear that the cross-over between the dark and light characteristics which occurs after heat treatment is much more pronounced from devices formed by the wet plating technique, although they showed no cross-over at all in the as-made condition. With the devices formed by the dry barrier process some cross-over occurs even in the as-made condition, although this is to be expected considering the thermal treatment necessary to form the Cu_xS layer. Another noticeable feature is the larger value of fill factor (0.7) for the wet plated cell compared with 0.6 for the dry barrier device. However, the OCV from dry barrier cells is larger, 0.54V compared with 0.48V, while the SCCs are comparable. The series resistances in wet plated cells were smaller than those of dry barrier cells, which correlates with the differences in the fill factors.

5.4.4 Spectral Response

Typical spectral response curves, showing OCV and SCC as a function of the wavelength of the incident monochromatic radiation for the as-prepared cell and for cells heated separately for 2, 7 and 10 minutes in argon and in air are shown in Figure 5.25 and Figure 5.26. In the as-prepared cell the maximum response of OCV occurred in two bands centred near 0.96 and 0.8 μm, with the former more prominent. These bands have been discussed in the previous section and are associated with the generation of electron hole pairs in the chalcocite ($Cu_{2.0}S$) and djurleite($Cu_{1.96}S$) phases of the copper sulphide layer[18]. The heat treatment in air led to a pronounced shift of the 0.8 μm peak to shorter wavelengths, so that after 7 minutes it was situated

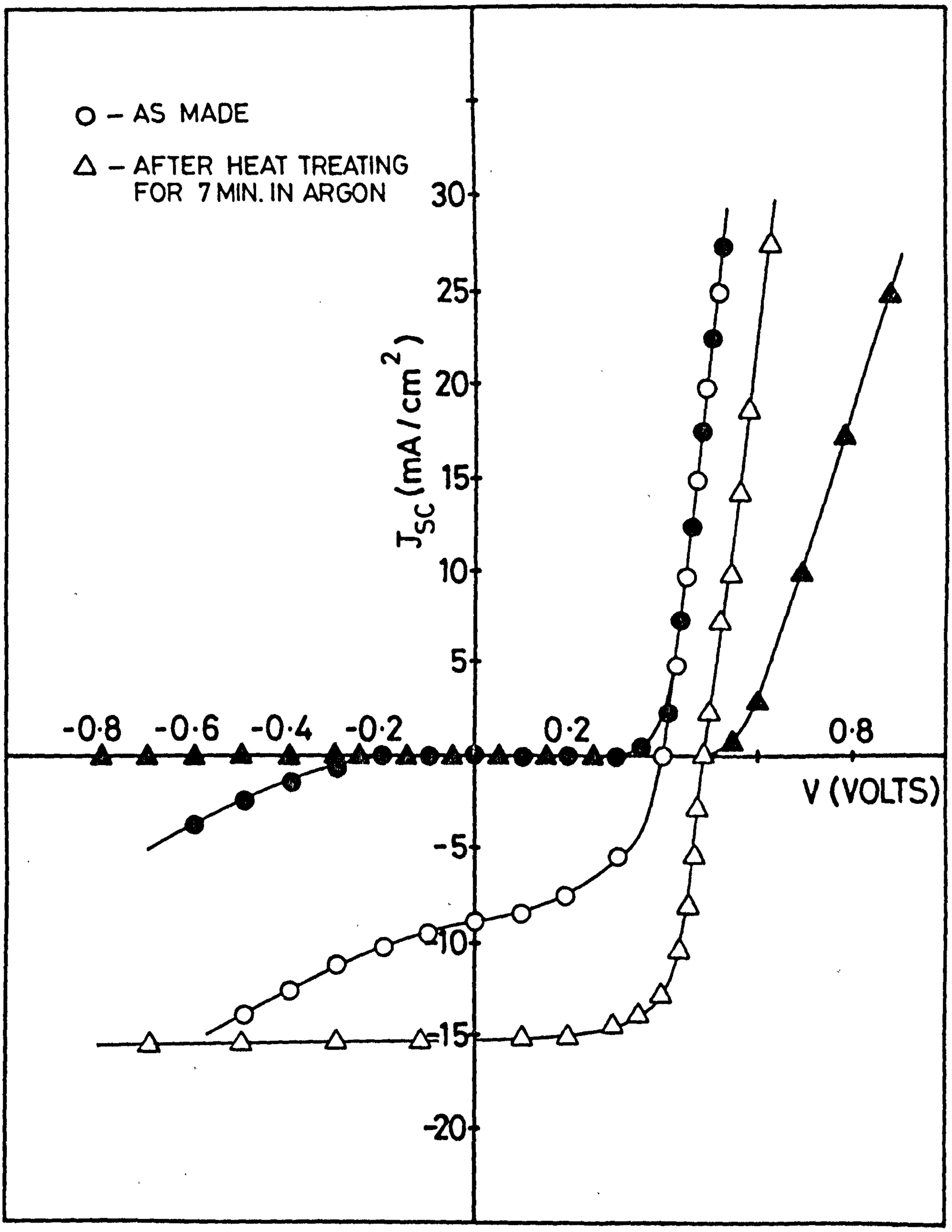


FIGURE 5.24: Current-voltage characteristics of a device prepared by the wet plating technique.

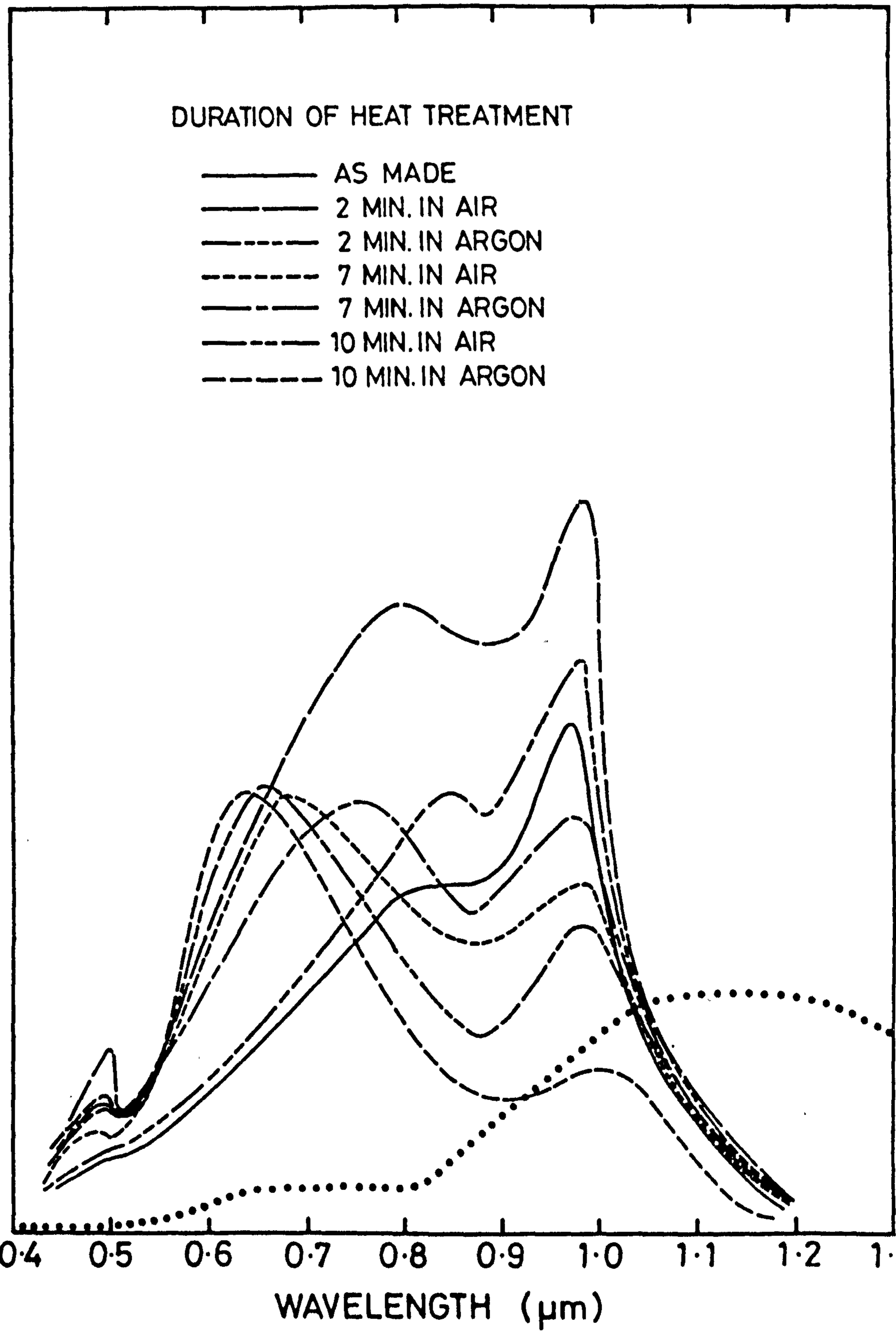


FIGURE 5.25: Spectral responses of the open circuit voltage of cells heat treated at 200°C in different ways.

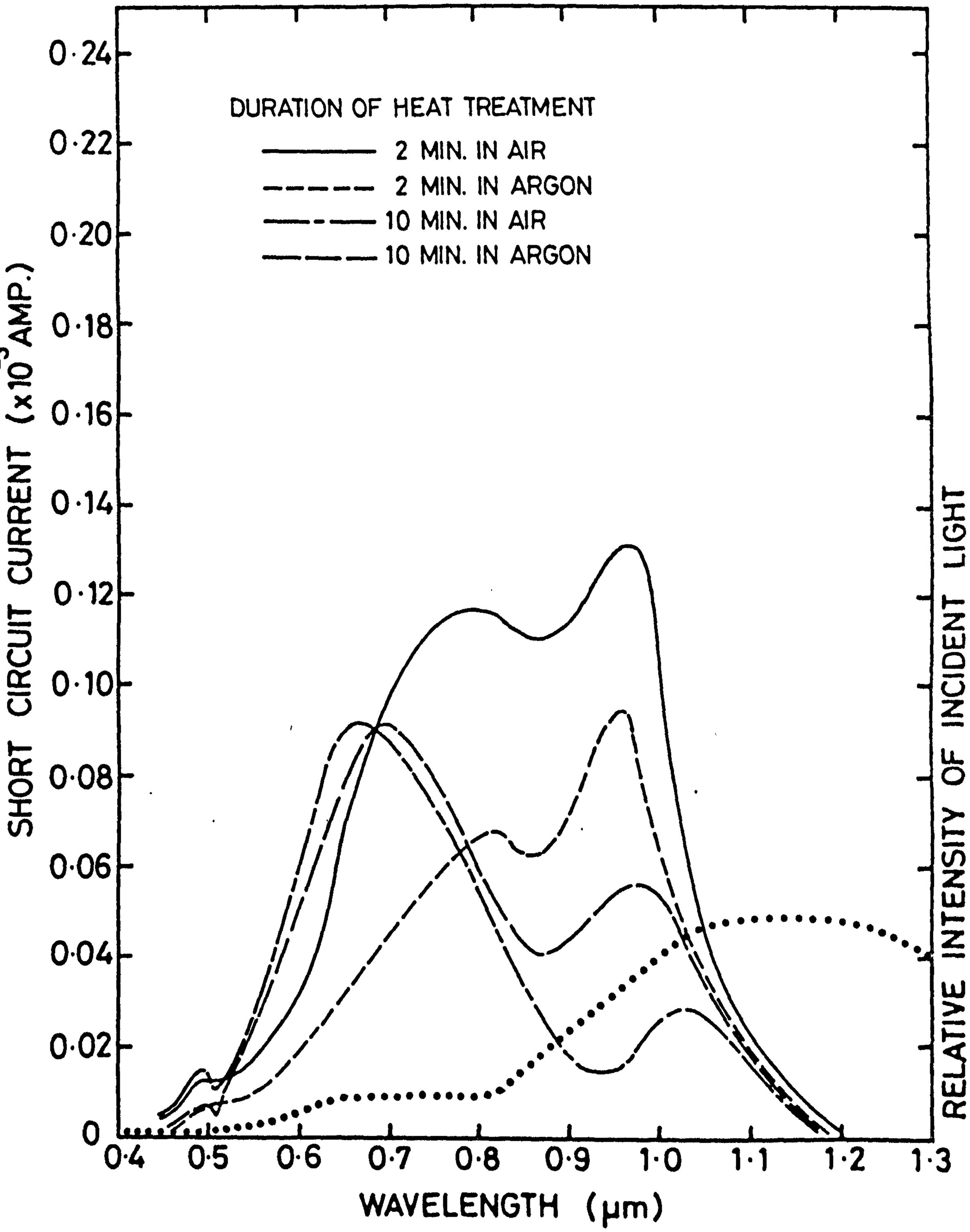


FIGURE 5.26: Spectral responses of the short circuit current of cells heat treated at 200°C in different ways.

at about 0.65 μm. The shift was also accompanied by a dramatic reduction in the speed of response to sudden changes in the wavelength of illumination, which suggests that it is attributable to increased excitation from copper acceptor levels within the depletion region of the CdS[18]. Heat treatment in argon led to a similar but less pronounced shift of the djurleite peak to shorter wavelengths. In addition heat treatments for 7 minutes in either air or argon led to the appearance of a small peak in the response at 0.5 μm at the band gap of CdS. In all the cells, the spectral response of SCC was similar to that of OCV (Figure 5.26).

The spectral response of the heat treated samples was also measured at 85K and the results are shown in Figure 5.27. It is obvious from the curves in this figure that the peak at 0.8 μm was more pronounced in the air baked device suggesting that more djurleite was formed after heating in air. Interesting results were observed for the sample heated in the H_2/N_2 for 7 minutes. At room temperature two peaks appeared near 0.96 μm and 0.65 μm, while at 85K a pronounced peak appeared at 0.96 μm and the response between 0.6 and 0.7 μm at room temperature diminished. Such behaviour has already been discussed in section 5.4. Following the ideas developed there the response at 85K can be attributed to the chalcocite phase while that at 0.65 μm at R.T. is due to copper in CdS.

5.4.5 Bias Illumination

The effect of bias light on the spectral response of the CdS cells was also studied before and after heat treatment. A device was illuminated from a secondary source with fixed intensity and wavelength (0.52 μm) while the spectral response was measured using the monochromator. The measured responses, with and without bias light, of an as-made device carrying a layer of the chalcocite are shown in Figure 5.28. The two spectral responses are quite similar although there was a slight enhancement near 0.96 μm, when bias light was used. With the air heated cell the peak at 0.68 μm without

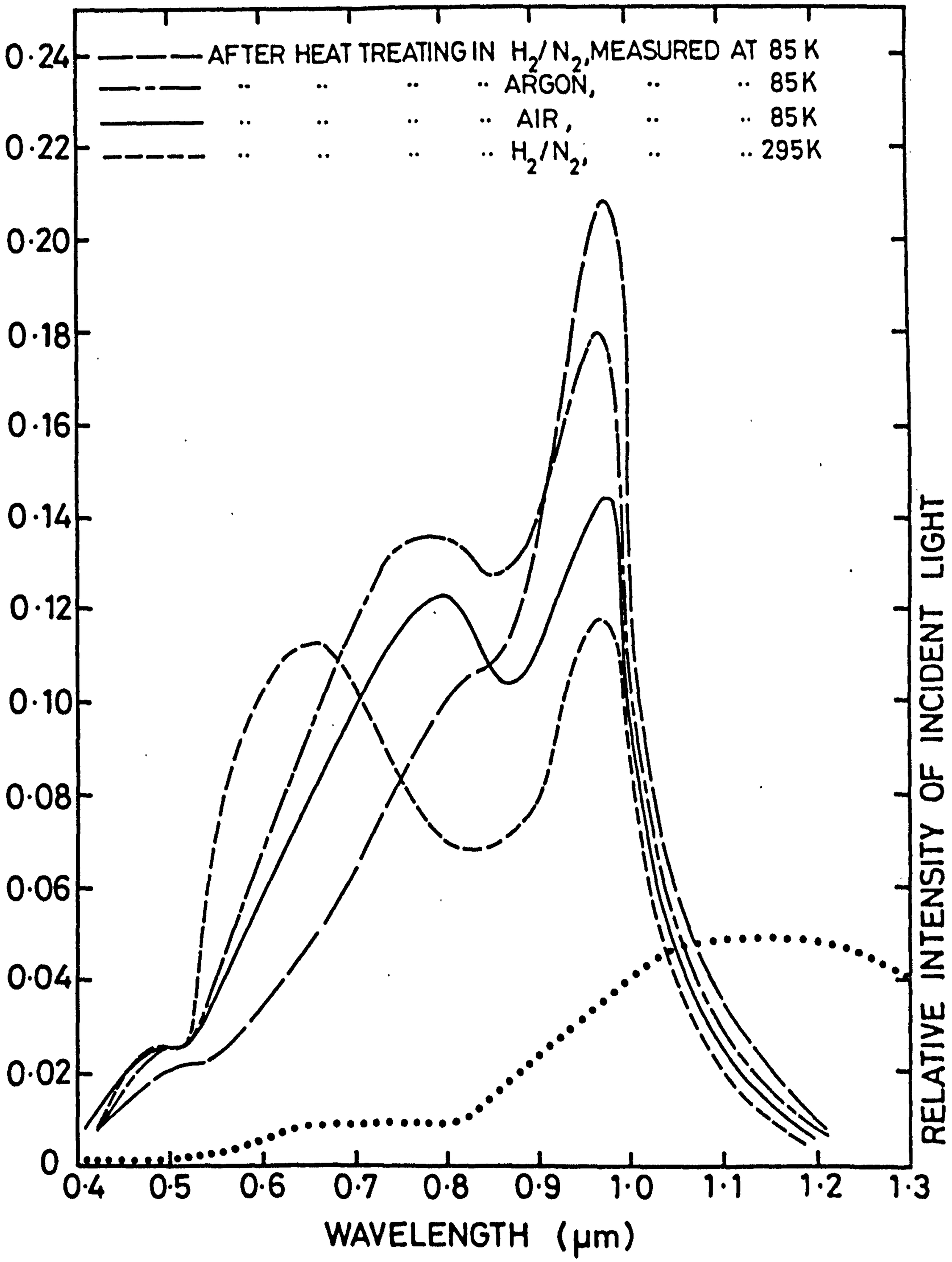


FIGURE 5.27: The dependence of spectral response of devices on the temperature of measurement and the ambient used for the heat treatment.

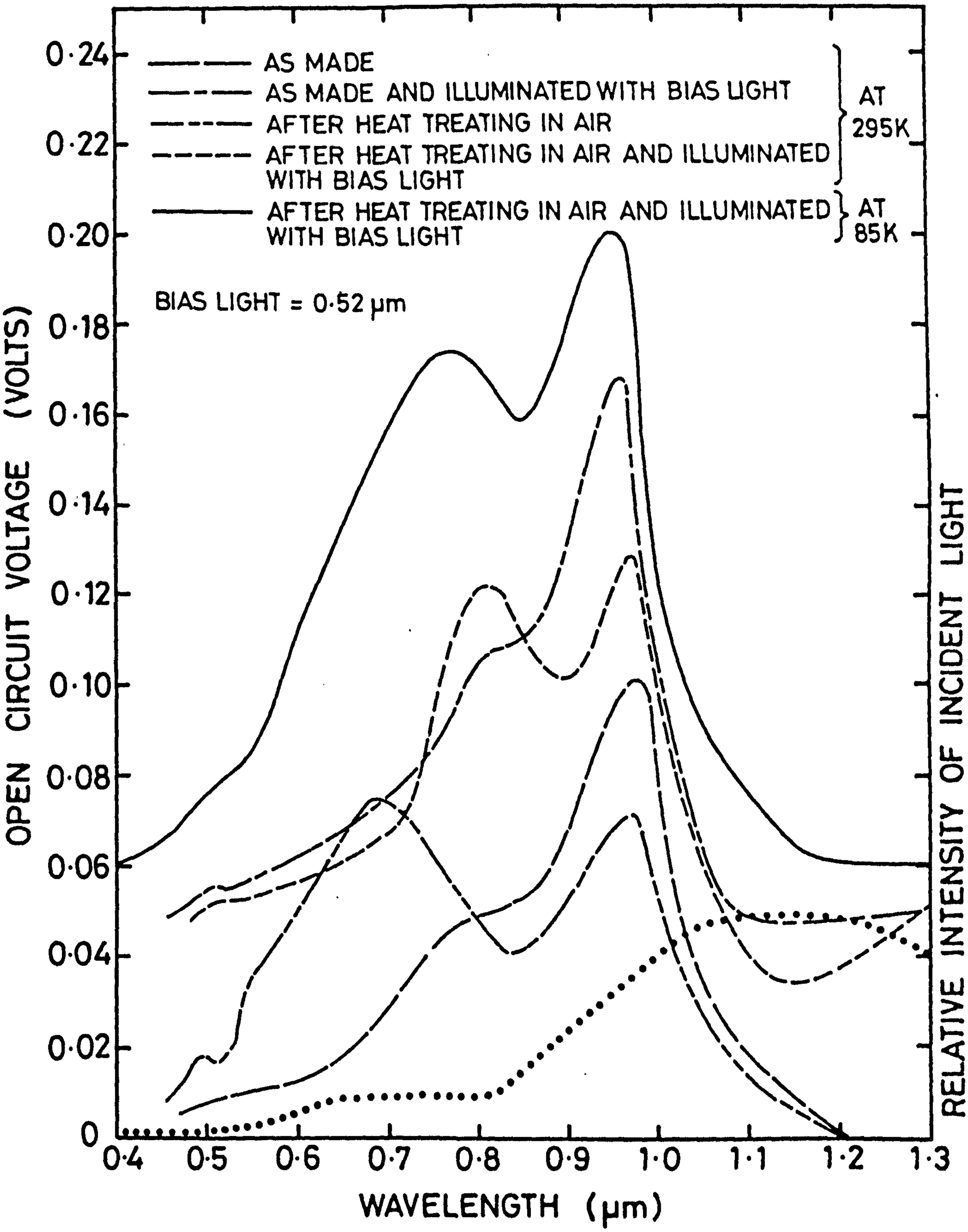


FIGURE 5.28: The effect of temperature and bias illumination on the spectral response of the cells heat treated in different ways.

bias light shifted to 0.8 μm with bias. The bias also caused slight quenching in the range from 1.1 to 1.3 μm.

The spectral response with bias light of a device prepared with a substrate temperature of 50°C is shown in Figure 5.29. In this device there was an enhancement in the sensitivity in the red region, while quenching was observed in the blue region. The spectral response of the cell heated in the H_2/N_2 mixture was also measured under bias light illumination. The normal response is shown in Figure 5.27. With bias light the red response near 0.9 μm increased slightly but the green response known to be due to copper in CdS was quenched. This quenching can be explained by considering that on illuminating with bias light the deep centres formed by the copper diffusion are filled with holes. Hence on illuminating with green light the excitation of electrons from these levels is no longer possible.

A quenching was also observed in the wavelength range from 1.1 to 1.3 μm. This feature can be attributed to the thermally assisted emptying process[29] which takes place with the superposition of infrared light. Since this quenching disappears at liquid nitrogen temperature, it further confirms that the process is thermally activated. It is important to mention that the response also depends on the relative intensities of the two sources.

5.5 DISCUSSION ON POST BARRIER HEAT TREATMENT

Te Velde[4] considered air baking to be an essential part of the process of preparing devices by the dry barrier method. According to him air baking promotes the adsorption of oxygen at the interface, which in turn determines the band bending in the adjacent CdS[41]. Moreover air baking for a short period does not significantly disturb the stoichiometry of Cu_xS layer[9]. However, Burton and Windwai[42] found deleterious effects on heating such devices in air, one of which was the change in the stoichiometry from chalcocite to djurleite caused by oxygen. In contrast, heat treatments

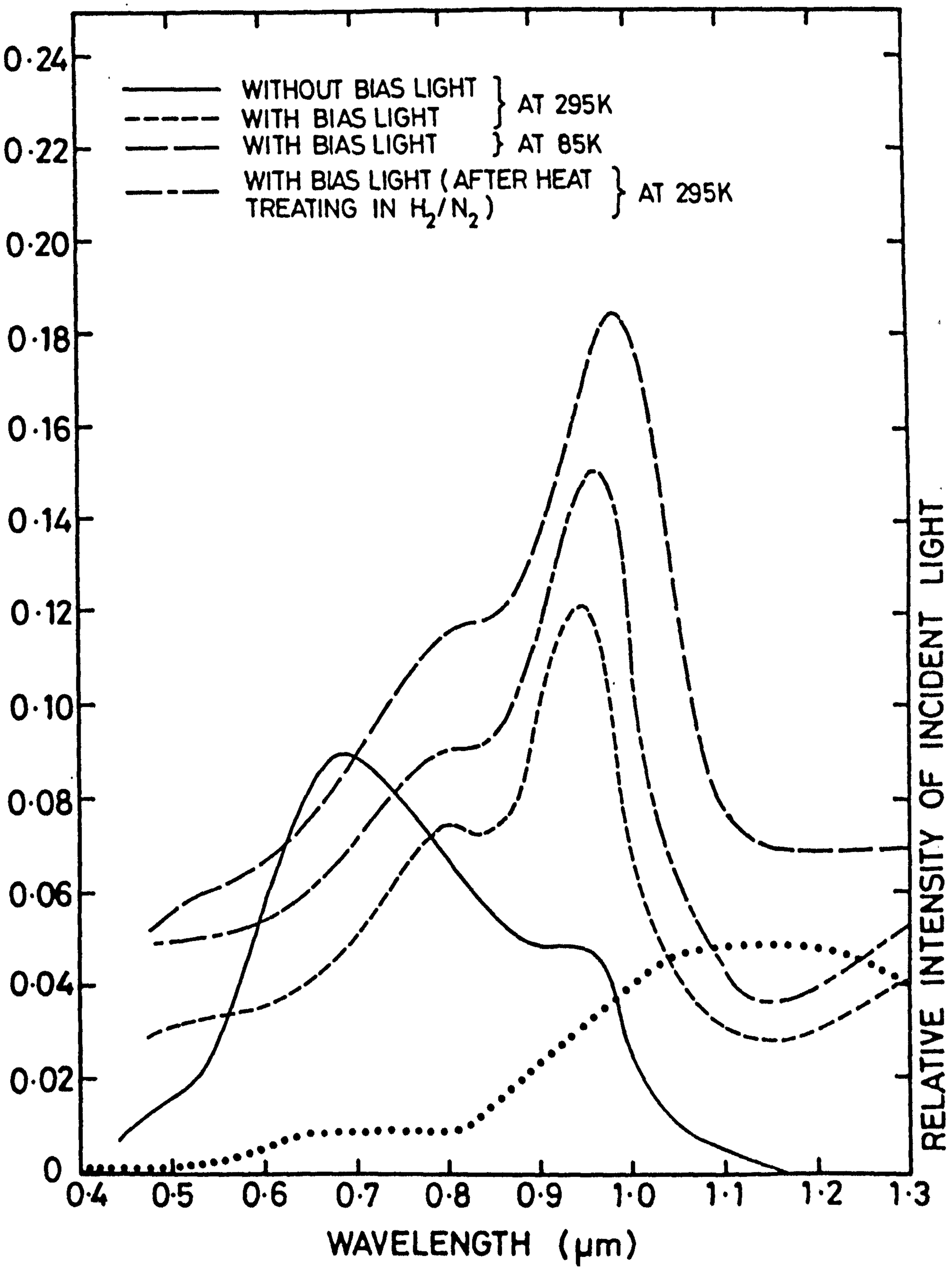


FIGURE 5.29: The effect of temperature and bias illumination on the device comprised of a chalcocite layer and Cu levels diffused into CdS.

in reducing atmospheres have the reverse effect and are beneficial[43]. Besides this another of the effects of heat treatment is the formation of a compensating i layer in the CdS produced by diffusion of Cu that effectively widens the space charge region[44,45]. This restricts the tunnelling of electrons from the CdS to the interface states, effectively increases the barrier and thus explains many of the device characteristics after heat treatment[46]. Moreover, the deep donor levels present in the CdS are also compensated[47]. All these processes have been found to change the field at the interface which in turn affects the interfacial collection factor and hence the efficiency of the device[45]. In addition the shunting paths are reduced[29].

The J-V characteristics in Figure 5.18 show that differences result from heating in air and in argon. With air baking the parameters OCV, SCC FF attain a maximum value at an earlier stage of the heat treatment. This difference may be attributed to the fact that in air heated devices the compensation at the interface takes place as a result of diffusion of copper as well as of oxygen which plays the role of electron acceptor[41]. With argon heated cells compensation is by the diffusion of copper only. However, the devices heated in air were inferior because of their poor fill factor. This was a consequence of the two shoulders which appeared in the J-V characteristics in the same positions as those reported by Boer[48] and attributed to deep donors in CdS at 0.6 eV and 0.22 eV below the conduction band. It appears that the formation of these defect levels is augmented by baking in air.

During heat treatment many processes may occur in addition to the diffusion of Cu into the CdS to form the i layer. Some Cd diffuses in Cu_xS[5,49,50,51]. This process is enhanced in the presence of oxygen[50,51,52]. An oxide layer may also form on the free surface of the Cu_xS causing deterioration in the stoichiometry[42], and a change in sheet resistance of the

Cu_xS layer[52]. All these processes would therefore affect the series resistance of the device. The net result therefore depends on the ambient and duration of annealing.

The effect of heat treatment on the stoichiometry of the Cu_xS layer was revealed by the spectral response measurements (Figures 5.25 and 5.26). It is clear that on heating the device in air for 2 minutes, the spectral response of the OCV improves despite the fact that the djurleite peak also appears. However prolonged heating causes the response at 0.96 μm to decrease and that at 0.68 μm to increase. This is attributed to loss of copper by diffusion into the CdS, which can be inferred from the increasing cross-over between the dark and light characteristics. With heating in argon, the short wavelength peak occurs at about 0.7 μm indicating a deterioration in the stoichiometry. The small peak which appears at 0.5 μm confirms this deterioration since the consequent reduction in the absorption coefficient of the Cu_xS[22] allows more light to pass to the CdS. On heating further the response near 0.68 μm increases, while that at 0.96 μm decreases, indicating further deterioration in the stoichiometry, which is reflected in an even larger response from the band edge of the CdS.

As discussed in section 5.4, the temperature dependence of the spectral response of the as-prepared devices provides a decisive method of identifying the phase of Cu_xS. As a result the effect of temperature on the spectral response of all the heat treated samples was studied (Figure 5.27). This revealed that after heating in air or argon a small peak corresponding to djurleite appeared at 0.78 μm. In contrast, with the sample heated in the H_2/N_2 mixture, the dominant peak was at 0.96 μm corresponding to chalcocite. The improved stoichiometry can be attributed to the loss of sulphur from the Cu_xS layer in the presence of H_2, thus increasing the copper content. Nevertheless the devices heated in H_2/N_2 had a peak at R.T. at 0.65 μm associated with copper acceptor levels in CdS[18]. This is quite expected because of the

diffusion of copper during heat treatment. In all cells the response from the copper acceptors diminished at 85K. As discussed in section 5.3.2 the short wavelength response at RT has been attributed to the excitation of electrons from the deep acceptor state to the conduction band while the holes are thermally freed to valence band. At lower temperature thermal freeing of holes does not take place and hence the green response diminishes.

In addition to this, the study of the spectral response with bias light (0.52 μm) revealed that the short wavelength response was quenched in the presence of bias light and the red response was dependent on the phases of Cu_xS. The enhanced red response may be due to the reduction in series resistance of the photoconducting i-layer on the application of bias light as described by Shiozawa et al[28]. Alternatively, it could be attributed to the depopulation of impurity levels by electron transitions resulting in additional minority carriers[53], since this process has been reported to increase the life time of free holes[54].

The effect of bias light illumination on the spectral response of the heat treated cell has also been explained as the modification of the normal response by the energy gate characteristics of the photoconducting layer[55]. Our results show that the effect of the bias light (0.52 μm) on the response in the short wavelength region is controlled by the photoconducting layer (as discussed in section 5.4.5) but the red response was still dependent on the dominant phase of Cu_xS. Thus in as-made devices the response peak was at 0.96 μm with bias light, showing the chalcocite phase of Cu_xS, while two peaks at 0.96 μm and 0.8 μm appeared in heat treated cells indicating the presence of chalcocite and djurleite. This also demonstrates that the photosensitivity of the device is dependent on the phase as observed by Kantariya et al[56].

From these observations it is apparent that heat treatment for periods up to 7 minutes in argon produces optimum J-V characteristics, though some copper diffuses from the copper sulphide into the CdS during this time

thereby affecting the stoichiometry adversely. In order to improve the stoichiometry, the samples can be exposed to a hydrogen glow discharge or a thin layer of Cu can be evaporated on to Cu_xS layer, followed by heat treatment in air[57,58]. These processes have been found to be effective for thin film cells, not only in improving the stoichiometry, but also in reducing the degradation of the device during continued operation. Our results show that the effect of a 100 Å copper layer was more pronounced when it was deposited on a Cu_xS layer which had been heated for 7 minutes in argon, i.e. the copper layer treatment is best administered after the device has been optimised. This might be explained by the fact that once the optimised device is obtained and the compensation at the interface is realized, further heat treatment with an additional layer of copper in the presence of oxygen simply improves the stoichiometry while a thin surface layer of Cu_2O is formed which acts as a minority carrier mirror[59].

5.6 CONCLUSION

The dry barrier process is an important technique for use in fabricating CdS - Cu_xS heterojunctions on very thin films[5]. It is well established that the phase of Cu_xS should be chalcocite if an efficient device is to be obtained. The work reported here has revealed that by carefully monitoring the preparational parameters, the phase of Cu_xS layer can be adjusted as required. The spectral response of these devices at low temperature (85K) gives more reliable information about the dominant phase of the Cu_xS since the response from the photoconducting i layer diminishes at 85K. Similarly with the application of bias light (0.52 μm) the response is controlled mainly by the phase of the Cu_xS layer. In those cases where post barrier heat treatments were investigated it was found that poor fill factors were obtained after heating in air. Thus most efficient devices were obtained after heating at 200°C in argon for 7 minutes. Further improvement in the SCC could be achieved by a final treatment with evaporated copper.

REFERENCES TO CHAPTER 5

1. G.J.Russell, A.T.Fellows, S.Oktik, E.Ture and J.Woods: Journ.Mat.Sci.Letters 1 (1982) p.176.

2. E.P.Warekois,M.C.Lavine,A.N.Marino,H.C.Gatos: J.Appl.Phys. 33 (1962) p.690; Erratum:J.Appl.Phys.37(1966) p.2203.

3. R.W.Smith: Phys.Rev.97 (1955) p.1525.

4. T.S.Te Velde: Energy Conversion 15 (1975) p.111.

5. A.N.Casperd and R.Hill: Proc.Photovoltaic Solar Energy Conf. Luxembourg, 1977, (Reidel-Dordrecht, 1977) p.1121.

6. M. Burgelman, A.Devos and L.Vandendriessche: Proc.Fifth E.C. Photovoltaic Solar Energy Conference, Athens, Greece, Oct.1983 (Reidel Dordrecht, 1983) p.873.

7. A.Rothwarf and H.Windawi: Proc.14th IEEE Photovoltaic Specialists Conf.San Diego, California, Jan.1980, p.722.

8. W.Palz, J.Besson,T.N.Duy and J.Vedel: Proc.9th P.V.Specialist Conf, Silver Springs, Maryland, May 1972. IEEE New York, 1972, p.91.

9. T.S.Te Velde and J.Dieleman Philips Res.Repts.28 (1973) p.573.

10. N. Nakayama, A.Gyobu and N.Morimoto: Jap.J.Appl.Phys. 10 (1977)p.1415.

11. N.Nakayama: Jap.J.Appl.Phys.B (1969) p.450.

12. R.Hill: in "Active and Passive Thin Film Devices" ed.by T.J.Coutts. (Academic Press, 1978), Chapter 10,pp.487 to 594.

13. W.F.Tseng and I.G.Greenfield: Phys.Stat.Sol.26 (1974) p.643.

14. H.C.Hadley and W.F.Tseng: J.Crystal Growth 39 (1977) p.61.

15. O.J.Cain and R.W.Vook: Thin Solid Films, 51 (1978), p.373.

16. G.J.Russell and J.Woods: Phys.Stat.Sol(a) 46 (1978) p.433.

17. W.R.Cook, L.Shiozawa and F.Augustine: J.Appl.Phys. 4 (1970), p.3058.

18. B.G.Caswell,G.J.Russell and J.Woods: J.Phys.D:Appl.Phys.8 (1975)p.1889.

19. B.G.Caswell, G.J.Russell and J.Woods: J.Phys.D:Appl.Phys.10 (1977)p.1345.

20. R.Marshall and S.S.Mitra: J.Appl.Phys.36 (1968)p.3882.

21. B.G.Caswell: Ph.D.Thesis. University of Durham, 1976.

22. B.J.Mulder: Phys.Stat.Sol(a) 13 (1972) p.79.

23. P.I.Fedorov and M.N.Shakova. Izv.Vyssh.Uchebn.Zaved,Khim Khim Tekhnol.4 (1961)p.550.

24. G.Krabbes and H.Opperman: Z Anorg.Allg.Chem.435 (1977)p.33.

25. L.D.Polyachenok,K.Nazarov and O.G.Polyachenok: Russ.J.Phys.Chem.51 (1977) p.323.

26. D.F.Brestovansky, B.N.Baron, R.E.Rocheleau and T.W.F.Russell: J.Vac.Sci.Technol.1 (1983) p.28.

27. J.Dieleman Proc.Int.Workshop on CdS Solar Cells and Other Abrupt Heterojunction, Delaware, (1975), p.92.

28. L.R.Shiozawa, F.Augustine,G.A.Sullivan, J.M.Smith and W.R.Cook: Aerospace Res.Lab, Rep.ARL.69-0155 (1969).

29. W.D.Gill and R.H.Bube, J.Appl.Phys. 41, (1970) p.3731.

30. P.F.Lindquist and R.H.Bube, J.Appl.Phys. 43 (1972) p.2839.

31. P.C.Pande, G.J.Russell and J.Woods, J.Phys.D: Appl.Phys.16 (1983) p.2307.

32. M.Burgelman et al : Solar Cells 8 (1983) p.33.

33. P.C.Pande, G.J.Russell and J.Woods: Proc.5th E.C.Photovoltaic Solar Energy Conf.Athens, Greece, Oct.1983 (Reidel Dordrecht,1983) p.171.

34. J.J.Wysocki and Paul Rappaport: J.Appl.Phys.31 (1960) p.571.

35. N.Miya: Jap.J.Appl.Phys. 9 (1970) p.768.

36. J.Morimoto: Memoires of the Defence Academy, Japan, Vol.XVII(4)(1977)p.171

37. C.H.Cheng, B.Merritt, C.W.Tu and K.A.Jones: Solar Cells 10 (1983) p.287.

38. S.Oktik, G.J.Russell and J.Woods: Solar Energy Materials 9 (1983)p.77.

39. R.J.Chaffin and G.C.Osbourn: Appl.Phys.Letter 37 (1980) p.637.

40. S.Oktik: Ph.d.Thesis, University of Durham, 1982.

41. T.S.Te Velde: Solid State Electronics 16 (1973) p.1305.

42. L.C.Burton and H.M.Windawi: J.Appl.Phys.47(1976) p.4621.

43. L.Hmurick ,L.Allen and R.A.Serway: J.Appl.Phys.53 (1982) p.9063.

44. J.IBWilson and J.Woods: J.Phys.D.Appl.Phys.5 (1972) p.1700.

45. A.Rothwarf: Solar Cells 2 (1980) p.115.

46. A.L.Fahrenbruch and R.H.Bube: J.Appl.Phys.45 (1974) p.1264.

47. W.G.Haines and R.H.Bube: IEEE Trans.Electron Devices, Vol.ED-27, (1980) p.2133.

48. K.W.Boer: Phys.Stat.Solidi(a) 66 (1981) p.11.

49. F.J.Bryant, A.K.Hariri and C.G.Scott: J.Phys.D.Appl.Phys.16 (1983)p.2341.

50. F.J.Bryant,A.K.Hariri, S.Salkalachan and C.G.Scott: J.Phys.D.Appl.Phys. 16 (1983) p.1755.

51. J.V.Florio, K.J.Malysik and F.G.Ramos: Proc.15th IEEE P.S.Conference IEEE, New York, 1981) p.793.

52. L. Hmurick and R.A.Serway: J.Appl.Phys. 53 (1982) p.9073.

53. N.Duc.Cuong and J.Blair: J.Appl.Phys.37 (1966) p.1660.

54. J.Woods and J.A.Champion: J.Electron Control 7 (1959) p.293.

55. A.E.Potter, Jr., R.L.Schalla, H.W.Brandhorst, Jr. and L.Rosenblum: Proc.7th P.V.S.C. (1968) p.62.

56. R.V.Kantariya, S.Yu Pavelets and G.A.Fedorus: Sov.Phys.Semicond 11 (1977) p.1237.

57. K.Bogus and S.Mattes: Proc.9th IEEE Photovoltaic Specialists Conf. IEEE New York, 1972), p.106.

58. W.H.Bloss and G.H.Hewig: Proc.14th IEEE Photovoltaic Specialists Conf. (IEEE New York 1980) p.287.

59. W.H.Bloss and F.Pfisterer: Proc.5th E.C.P.S.E.C., Athens, Greece (Reidel-Dordrecht 1983) p.728.

CHAPTER 6

INTERFACE EFFECTS IN CdS/Cu_2S AND $Cd_{1-y}Zn_yS/Cu_2S$ PHOTOVOLTAIC CELLS

6.1 INTRODUCTION

In the fabrication of CdS/Cu_2S photovoltaic devices, post barrier heat treatment is normally administered in order to improve the performance of the device. In this process of heating, copper from the Cu_2S layer diffuses into the CdS and forms deep acceptor levels which affect the device performance[1-6]. In addition to this, the ambient in which the cells are heated also affects the device characteristics[7-9]. This has been discussed in detail in the preceding chapter where it was demonstrated that devices heated in air had poor fill factors compared to those of devices heated in argon. To account for this difference, effects occurring at the interface and in the depletion region of the CdS during the heat treatment have been investigated using the technique of infrared quenching of photocapacitance[10]. The copper profile in the CdS has been measured in the cells heated in oxidising and reducing atmospheres, and is discussed in this chpater. Even after optimum heat treatment the efficiency of CdS/Cu_2S cells is limited as a result of the lattice mismatch and difference in the electron affinities between the two semiconductors. These parameters primarily restrict tho maximum open circuit voltage which can be obtained[11]. Palz et al[12] were the first to propose the use of $Cd_{1-y}Zn_yS$ to overcome these difficulties and since then attempts have been made using various forms of $Cd_{1-y}Zn_yS$. Although the expected high values of OCV of cells fabricated on $Cd_{1-y}Zn_yS$ have been realised in evaporated layers[13-15], single crystals[16,17] and layers produced by spray pyrolysis[18-20], the values of SCC obtained so far have been disappointing in all types of cell. In order to investigate this problem, a study has been

carried out on the heterojunction formed using the dry barrier process on single crystal substrates of $Cd_{1-y}Zn_yS$ with composition $0 < y < 0.3$. Measurements of current voltage characteristics, spectral response and photocapacitance were carried out to study the processes occurring at the interface which affect the efficiency of the junction.

6.2 INFRA-RED QUENCHING OF PHOTOCAPACITANCE

The CdS/Cu_2S devices used were fabricated by the dry barrier process, as described in Section 5.2.2. Post preparative heat treatments were carried out in air, argon or a H_2/N_2 (60:40) mixture at 200°C for a period of 2 to 10 mins. The dark capacitance of each device was relatively large, and this had to be compensated so that the small changes induced by the monochromatic radiation, i.e. the photocapacitance, could be determined more accurately. Much of the investigation was concerned with a study of the infra-red quenching of the photocapacitance. For this the junction was first illuminated with a primary bias light with a wavelength close to the absorption edge of CdS. This was obtained by passing the light from a 250 W tungsten halogen lamp through an Oriel broad-band filter centred at 5200 Å. When an additional secondary radiation from the monochromator was allowed to fall on the device, the capacitance changed to a new steady state value in a time of about a minute. At longer wavelengths of the secondary radiation the capacitance was reduced, and this is what is referred as infra-red quenching of photocapacitance. The capacitance transients were recorded when the secondary radiation was switched on and off. The spectral response of infra-red quenching of photocapacitance was made by recording the transients as the wavelength of the secondary illumination was changed from long wavelengths to short wavelengths.

The curves in Figure 6.1 illustrate the infra-red quenching of the photocapacitance for three different devices, which had been subjected to post preparative heat treatment at 200° C for 7 min in argon, air or a 60:40

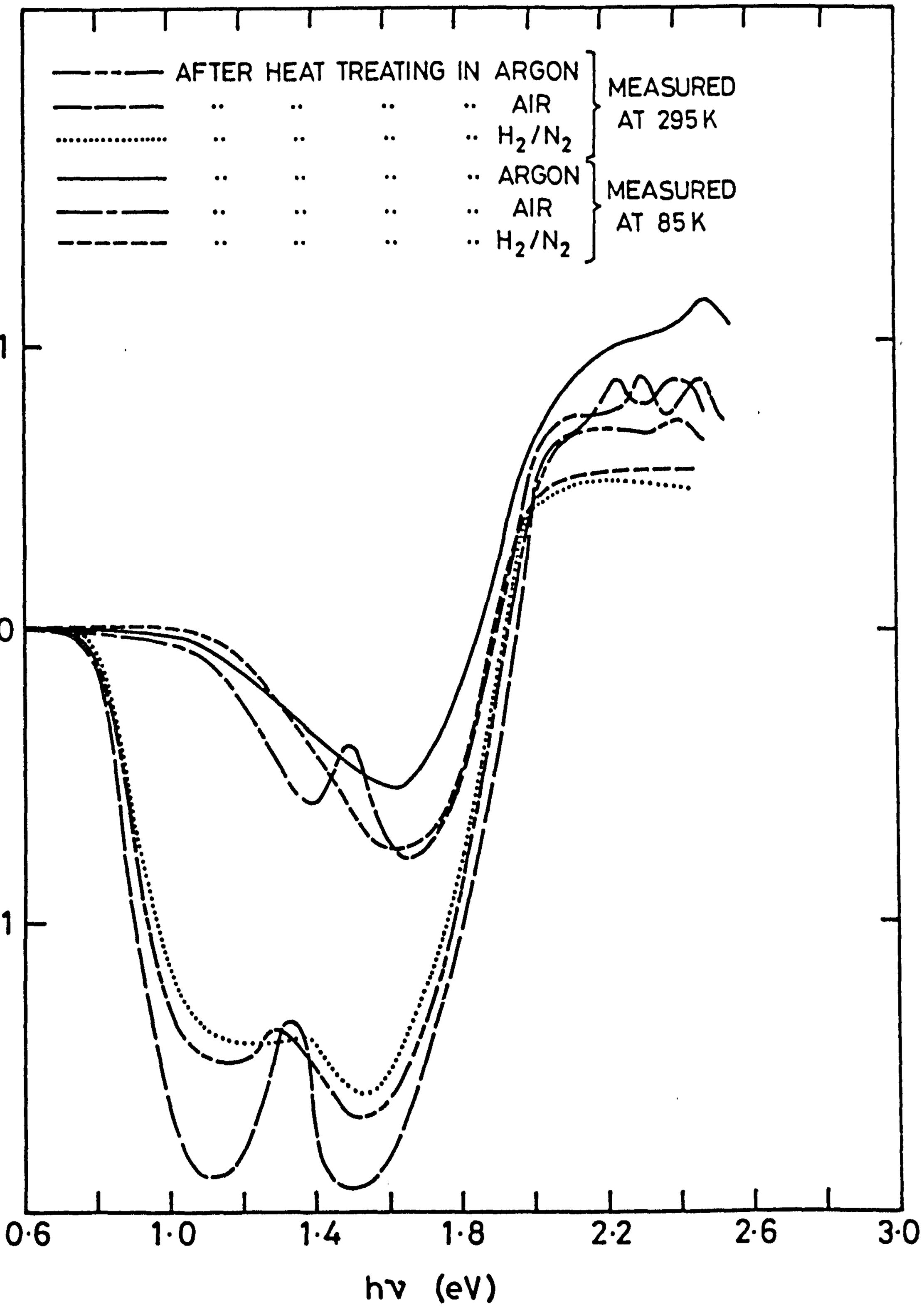


FIGURE 6.1: Infrared quenching of the photocapacitance of cells heated for 7 min at 200°C in air, argon and a hydrogen-nitrogen mixture.

mixture of hydrogen and nitrogen. Measurements were made at temperatures of 85 and 295 K for each device.

When a device was irradiated with primary light which excited electron-hole pairs across the band gap, the dark capacitance was increased substantially. This increase in capacitance was maintained after the primary excitation was removed. It is attributed to the capture of free holes into the ground state of the copper acceptors which becomes $(3d^9)$ Cu^{2+}. The electrons are swept away in the field of the depletion region and the increased trapped positive charge leads to an increase in capacitance. Since the ground state of the copper acceptor is very deep ($\sim$ 1 eV) thermal processes are negligible and the positive charge remains trapped when the primary excitation is removed.

The three lower most curves in Figure 6.1 show what happened when the devices, which were being held at room temperature, were simultaneously illuminated with the band gap bias light and with monochromatic secondary radiation, the wavelength of which was reduced after each transient was recorded. The measurement sequence was as follows.

The bias illumination was maintained continously. Once the steady state was reached the monochromatic secondary illumination was switched on, and the capacitance transient recorded until the new steady state was reached. The secondary illumination was then removed and the recovery transient was measured. Once the original steady state was reached the wavelength of the secondary radiation was reduced and the experiment repeated. The curves in Figure 6.1 show the total change in photocapacitance recorded at each wavelength of the secondary illumination.

The curves of Figure 6.1 show that there was a threshold for quenching of the photocapacitance at room temperature at 0.75 eV with all three devices. Moreover, when the experiment was repeated at 85K the threshold had shifted to about 1.1 eV. A similar effect was reported by Lindquist and Bube[2]. The quenching at 85K is attributed to the excitation of an electron from the valence

band to the ground state of the Cu^{2+} acceptor. The holes thus freed to the valence band are swept to the interface by the field of the depletion region. The net result is that the positive charge trapped in the depletion region decreases so that the capacitance decreases. At room temperature, quenching can occur at lower energy because the hole trapped in the ground state of Cu^{2+} can be raised to an excited state 0.75 eV below the ground state. The hole is then sufficiently close to the valence band for it to be thermally ionized at room temperature, again with the net result that the capacitance is reduced as the net positive charge on the Cu^{2+} acceptor is decreased. Since the threshold for quenching at room temperature was 0.75 eV, whereas the threshold at 85K was at 1.1 eV , it follows that the hole excited state lies 0.35 eV above the valence band (see Fig 6.2). With deccreasing wavelength of the secondary illumination, the quenching of the photocapacitance began to decrease and eventually the secondary radiation led to an enhancement of the (positive) capacitance. This is attributed to the increasing importance of direct excitation of electrons from the copper levels (not all of which would be filled with holes) to the conduction band. This begins to occur at about 1.5 eV at room temperature and 1.65 eV at 85K. The sum of the threshold energies for quenching and enhancement should, according to this agreement, be roughly equal to the band gap. In fact the sum at 85K was 2.75 eV which is slightly too large. The discrepancy could however be attributable to Frank Condon effects.

Additional structures were observed (Fig 6.1) in the photocapacitance curves of the device which had been heated in air. For example the downward trend in the quenching curve measured at 85K was arrested temporarily when the photon energy of the secondary illumination reached 1.4 eV, and a small maximum developed at about 1.55 eV. It is suggested that this is due to the excitation of electrons from the ground state of the copper acceptor to empty acceptor-like states at the interface between the Cu_xS and CdS, which lie

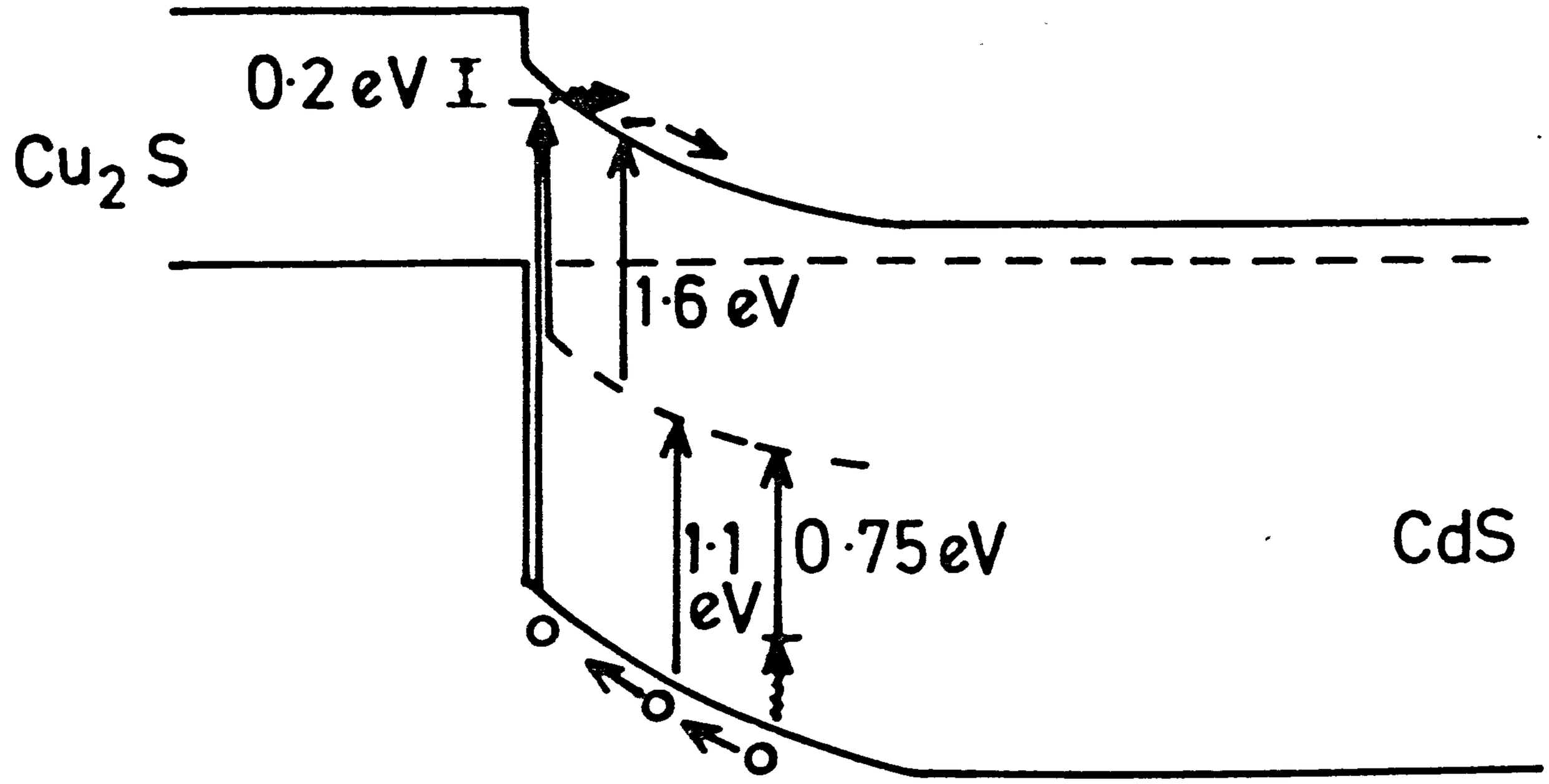


FIGURE 6.2: Energy band diagram at zero bias illustrating the various quenching and enhancing transitions.

approximately 0.2 eV below the conduction band of the CdS. The electron could then tunnel to the conduction band of the CdS leaving behind a hole trapped at Cu^{2+}, which would arrest the quenching process. The small maximum in the photocapacitance curve for the air treated device at 2.5 eV is almost certainly associated with additional bandgap excitation in the CdS. The feature at 2.3 eV may well be associated with a transition from the valence band of the CdS to the same interface states 0.2 eV below the conduction band. Such a transition would again lead to the loss of the electron by tunnelling from the interface state to the conduction band, while the free hole would be available to be trapped at the ground state of the copper acceptor. The fact that the two features under discussion were most prominent in the device heated in air, suggests if the interpretation is correct, that the interface states are associated with oxygen.

6.3 COPPER PROFILE

According to Suda and Bube[10] the concentration of copper centres, $N_T(w)$, at a depth w below the interface, is given by

$$N_T(w) = N_n(w) \left[1 - \left(\frac{dw_o}{dw_s} \right) \left(\frac{C_s}{C_o} \right)^3 \right] f_t^{-1} \qquad (6.1)$$

where $N_n(w)$ is the compensated donor concentration, C_o is the photocapacitance due to the primary light, C_s is the photocapacitance due to the secondary light and f_t is the occupation function given by [21]

$$f_t = \frac{\tau_{on}^{-1} - \tau_{off}^{-1}}{\tau_{on}^{-1}} \qquad (6.2)$$

where τ_{on} and τ_{off} are the time constants of the capacitance transients when the secondary illumination is switched on and off. $\frac{dw_o}{dw_s}$ represents the

incremental change in C_o with respect to that in C_s for a small change in bias voltage. Since

$$\frac{dC_o}{dC_s} = \frac{dC_o}{dV} \cdot \frac{dV}{dC_s} \tag{6.3}$$

it can be determined by measuring the two quantities on the right-hand side of equation 6.3. The magnitude of $N_n(w)$ can be obtained from the slope of the plot of C_o^{-2} versus V

$$N_n(w) = \frac{C_o^3}{\epsilon_o \epsilon_s q A^2} \left(\frac{dC_o}{dV} \right)^{-1} \tag{6.4}$$

and w is derived from the relation ship between the depletion width and junction capacitance

$$W = \frac{\epsilon_o \epsilon_s A}{C_o} \tag{6.5}$$

where ϵ_o and ϵ_s are the permittivity of free space and dielectric constant of the specimen respectively. Using values derived in these ways it was possible to calculate the concentration of copper acceptors at a variety of depths below the interface.

The logarithmic plots of the transients of the photocapacitance quenching and the recovery when the infrared light (1.1 eV) was switched on and switched off are shown in Fig. 6.3.

These linear semilog plots indicate a single time constant for the process of infrared quenching (τ_{on}) as well as for the recovery of the photocapacitance (τ_{off}). The occupation function calculated from the values of τ_{on} and τ_{off} by using equation 6.2 was found to be 0.62. This factor actually shows that the electron capture probability, under illumination with the secondary light, is not unity so that multiplying the RHS of

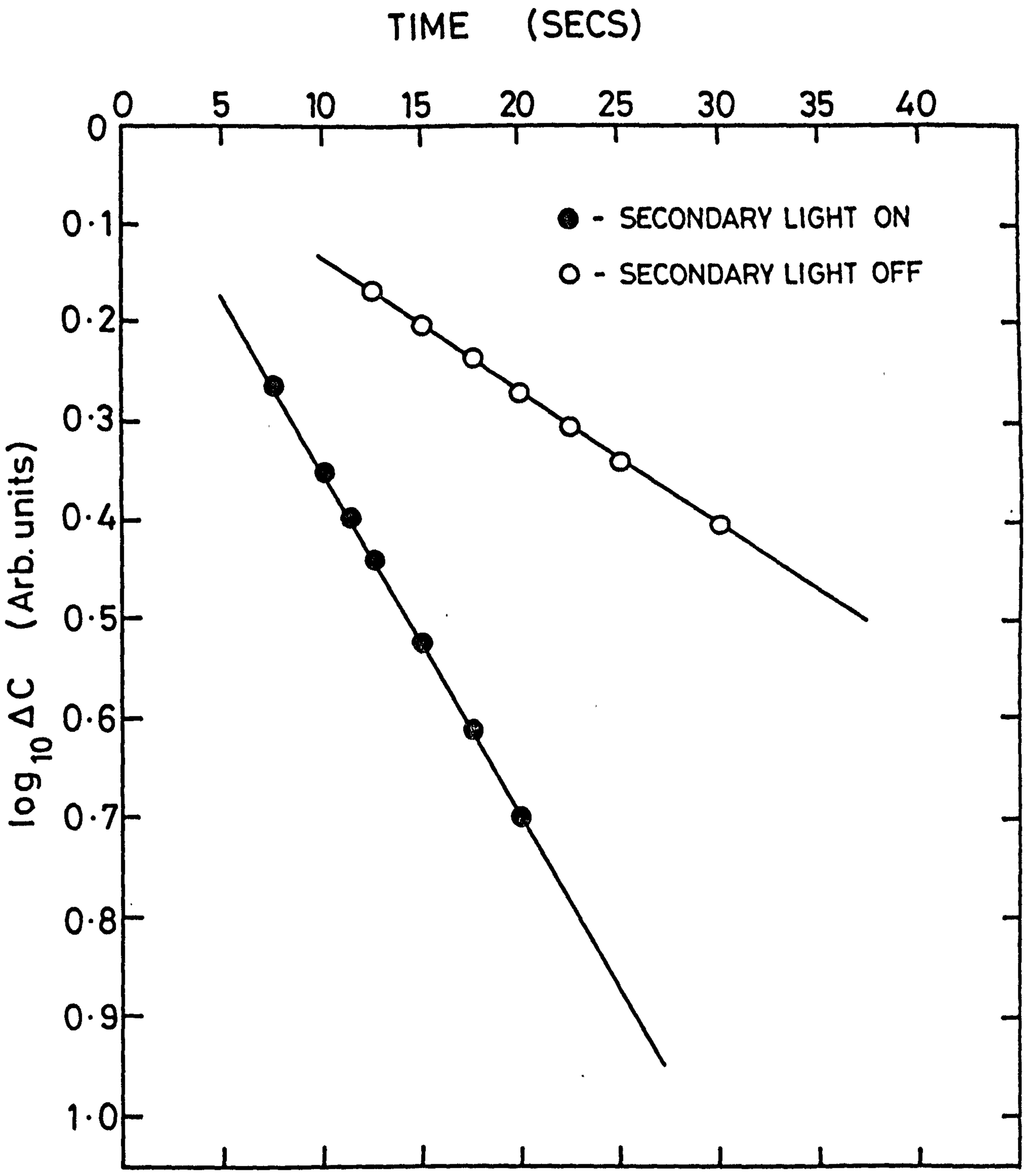


FIGURE 6.3: Logarithmic plots of the transients of quenching and recovery of the photocapacitance (at 85 K) when infrared light (1.1 eV) was switched on and off.

Eq. 6.1 by f_t^{-1} provides a corrected value of the deep centre concentration (21). The results obtained for the devices heated in air, argon and H_2/N_2 mixtures are shown in Fig 6.4. Since the measurements were made in reverse bias, only a limited range of the profile could be explored. Surprisingly most unusual distributions were revealed. Devices heated in air all showed minima in the profile, while those heated in argon exhibited pronounced maxima. Devices heated in a reducing mixture of hydrogen and nitrogen had profiles resembling those of devices heated in argon. The copper profiles in the as-prepared devices were much more normal in that the concentration was fairly constant over the range of values of w it was possible to measure.

6.4 INTERFACE EFFECTS IN DEVICES FORMED ON $Cd_{1-y}Zn_yS$

6.4.1 Preparation of the Device

The effects occurring at the interface were further investigated in the heterojunction on single crystals of $Cd_{1-y}Zn_yS$ grown by vapour phase technique . The details of the growth of the single crystal have been described in Chapter 4, Section 4.2 . For this the $Cd_{1-y}Zn_yS$ crystals were aligned using X-ray back reflection. Slices (2 mm thick) were cut with their large area faces perpendicular to the c axis and then mechanically polished in the same way as the CdS single crystals. Dice with dimensions 4 x 4 x 2 mm^3 cut from the slice were then used in the preparation of the device. The dice were etched for 20 secs in Conc.HCl and then indium ohmic contacts were applied to the Cd faces. The dice were etched for a further 10 secs before the CuCl was evaporated. The heterojunctions were formed as described in Chapter 5, Section 5.2.2. A layer of 0.2 μm CuCl was vacuum evaporated onto the sulphur faces of all the dice at a constant rate of 400 Å/min, while the dice were maintained at 35°C. They were then heated in argon at 200°C for 2 to 6 min to ensure that the solid state reaction between CuCl and $Cd_{1-y}Zn_yS$ was completed. An evaporated gold dot 1 mm in dia. was deposited on the copper sulphide layer for the second electrode.

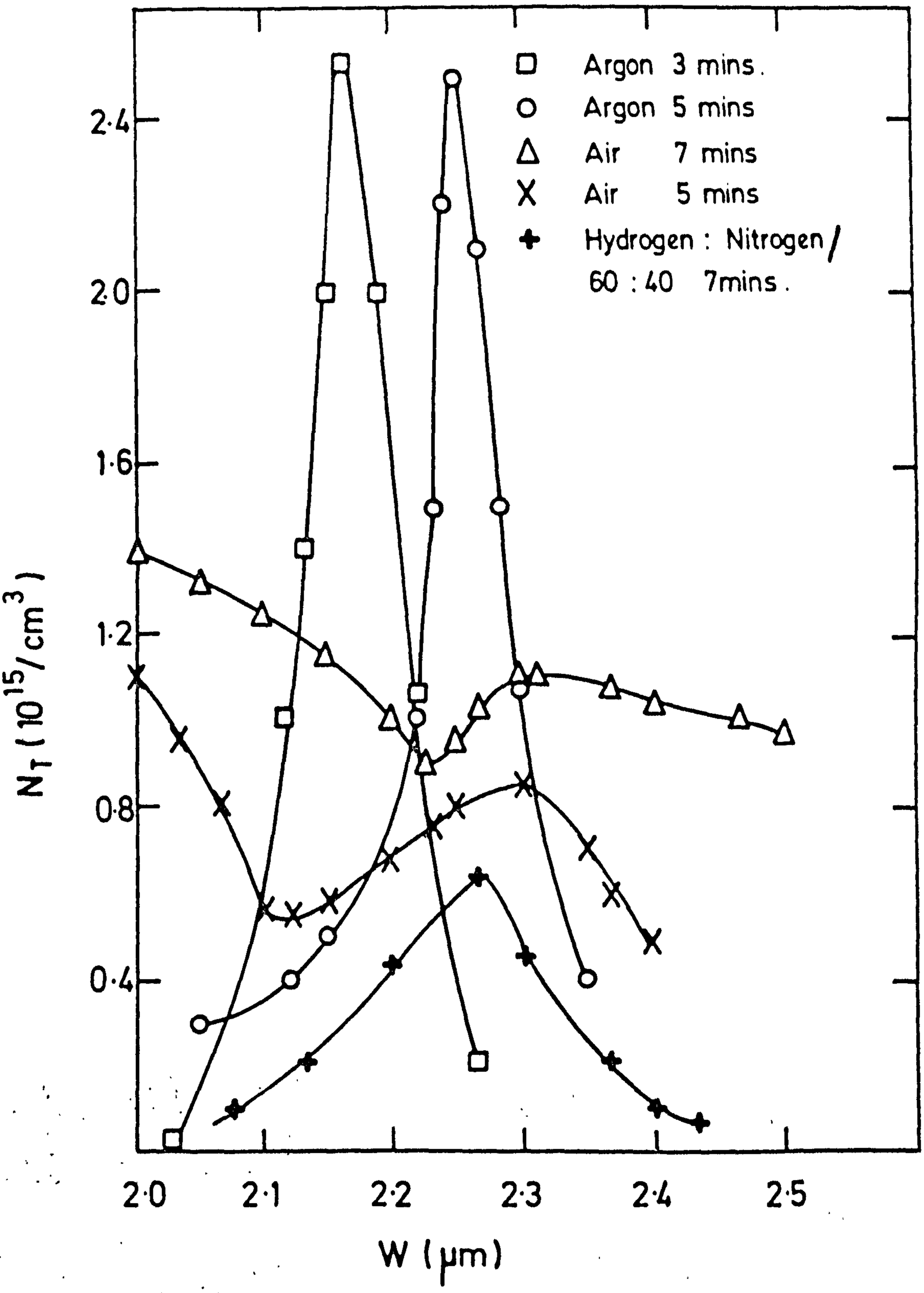


FIGURE 6.4: Copper concentration as a function of depth W below the interface for cells treated in various ways.

6.4.2 Cell Performance

It was noticed that the reaction between CuCl and $Cd_{1-y}Zn_yS$ proceeds slowly. The spectral responses of the OCV of the heterojunctions formed on $Cd_{0.8}Zn_{0.2}S$ by heating the sample for different lengths of time at 200°C in argon are shown in Fig 6.5. The measurements of the spectral responses were made at L.N. temperature to compare the performance of these devices, as our earlier studies on temperature dependence of spectral response have revealed that a more accurate assignment of the phase of Cu_xS could be made at L.N. temperature (see Section 5.3.2). It is evident from the curves of Figure 6.5 that the device heated for 2 min gives an inferior response compared to that heated for 4 min. The predominant peak in both curves occurs at 0.96 μm which corresponds to the chalcocite phase. The device formed after heating for 6 min also had its major peak at 0.96 μm but in addition a comparable response appeared at 0.78 μm. This shows that a mixture of chalcocite and djurleite was present in this Cu_xS layer. On the basis of these observations, a 4 min heating time was chosen to complete the solid state reaction on $Cd_{1-y}Zn_yS$ substrate.

The optical responses of devices formed on $Cd_{0.8}Zn_{0.2}S$ and on CdS are compared in Fig 6.6, which reveals that the red response is larger with the $Cd_{1-y}Zn_yS$ device. The dominant peaks at 0.96 μm at room and L.N. temperature for both the devices show that chalcocite is the predominant phase in the Cu_xS layer. The phase of the Cu_xS was also confirmed by RHEED patterns.

The spectral responses of devices formed on $Cd_{0.7}Zn_{0.3}S$ substrates by wet and dry processes were measured at L.N. temperature and are shown in Fig 6.7. It is obvious that the cell formed by the dry barrier process had a predominant peak at 0.96 μm while the cell formed by the wet process had an additional peak around 0.78 μm. This shows that the cell prepared by the dry barrier process had a higher chalcocite content.

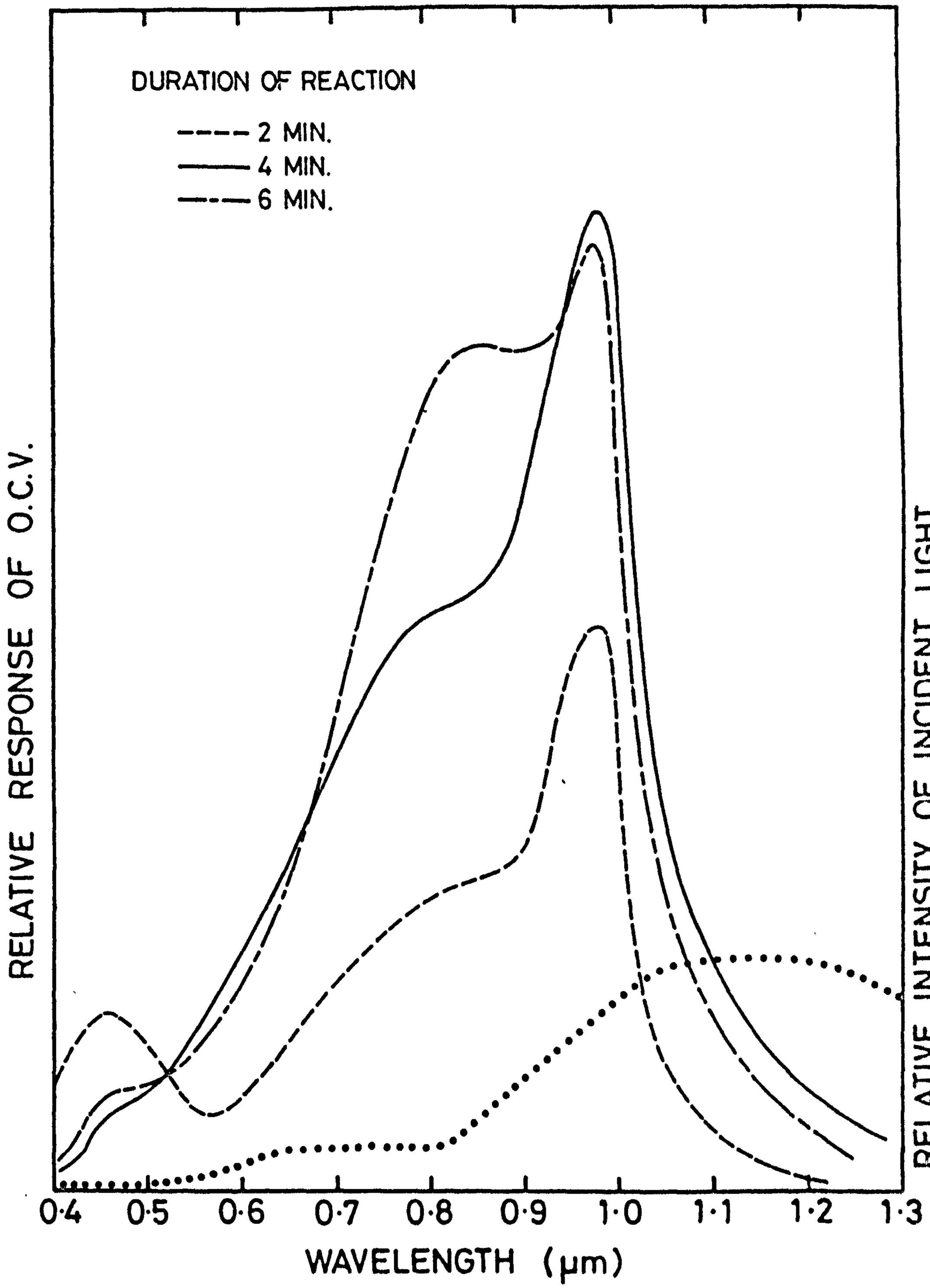


FIGURE 6.5: Spectral response of heterojunctions (at 85 K) formed on $Cd_{0.8}Zn_{0.2}S$ single crystal substrates after varying the duration of the reaction process.

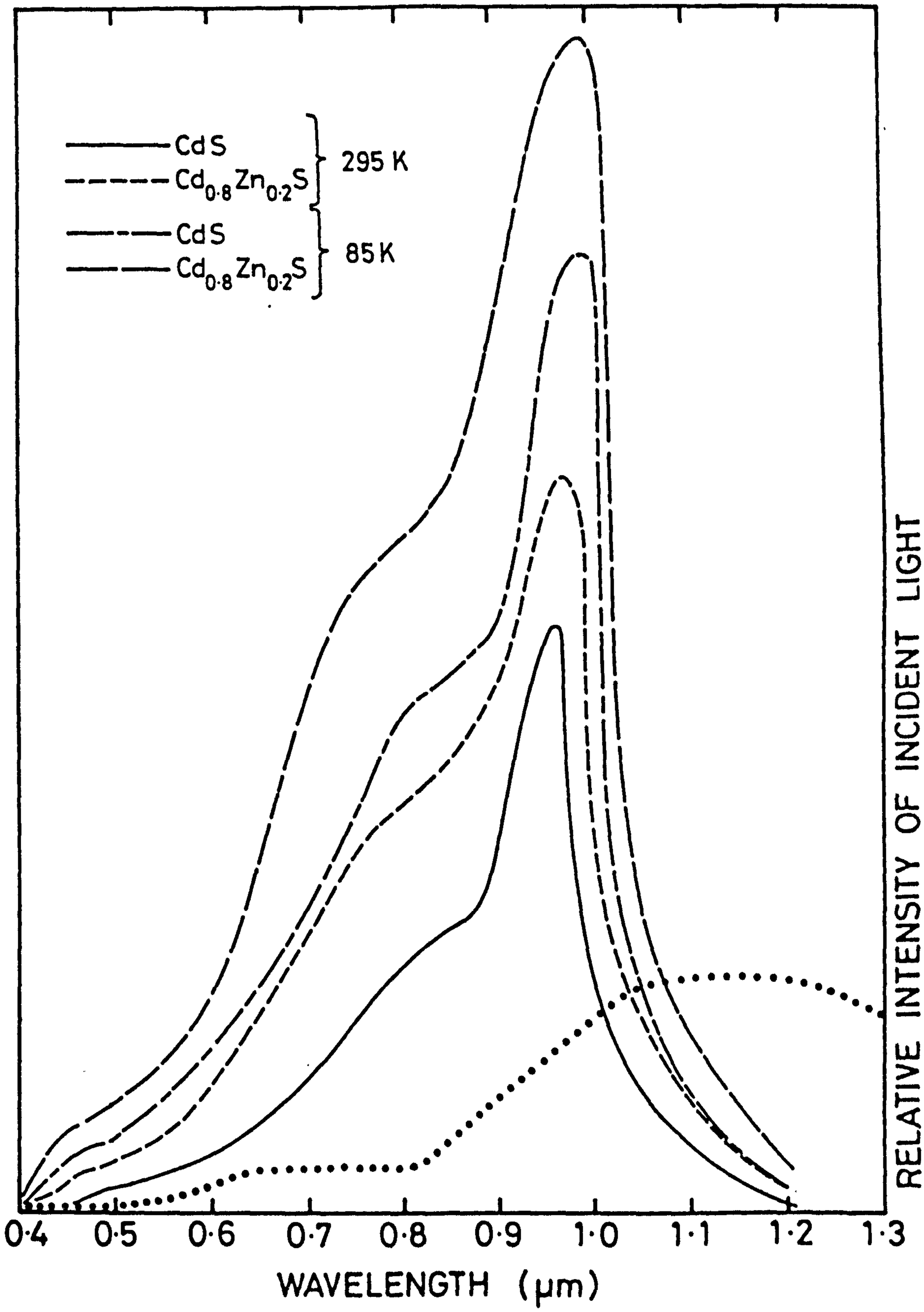


FIGURE 6.6: Temperature dependence of the spectral response of cells formed on $Cd_{0.8}Zn_{0.2}S$ and CdS single crystal substrates by the dry barrier process.

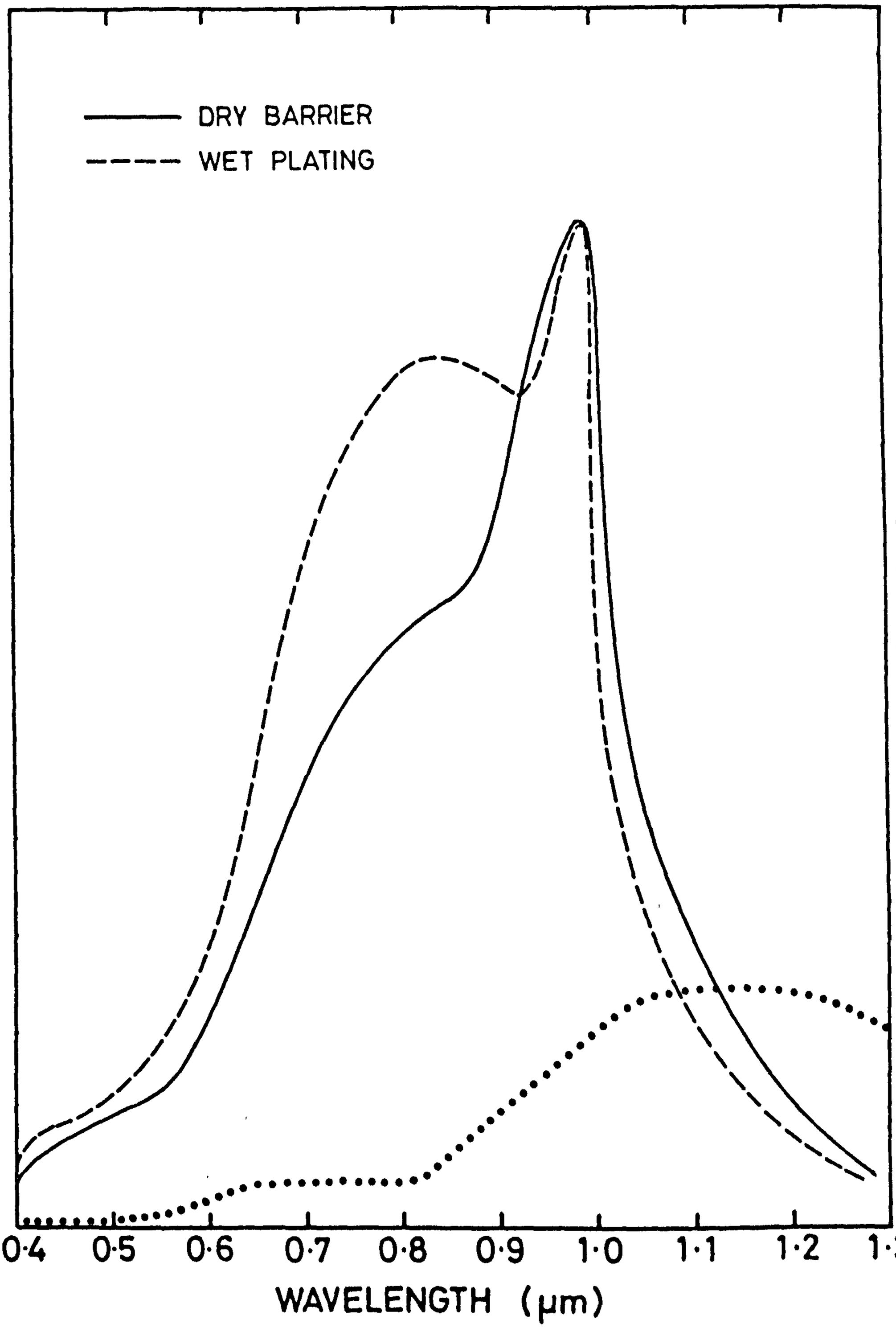


FIGURE 6.7: A comparison of the spectral responses of the hetero-junctions formed on $Cd_{0.7}Zn_{0.3}S$ by the wet plating and dry barrier processes.

The current voltage characteristics (in the dark and under AM 1 illumination) of heterojunctions formed on $Cd_{0.8}Zn_{0.2}S$ and CdS are shown in Fig.6.8. The effect of the inclusion of zinc in the CdS is to increase the OCV from 0.51V to 0.6V and to decrease the SCC from 15.5 mA/cm^2 to 12 mA/cm^2. It is worth noting that there was practically no difference in the fill factors. The device parameters obtained on the substrate of the various composition are as follows:

TABLE 6.1: Performance of Cells formed on CdS and $Cd_{1-y}Zn_yS$ Substrate

Cell Parameter	CdS/Cu_2S	$Cd_{0.9}Zn_{0.1}S/Cu_2S$	$Cd_{0.8}Zn_{0.2}/Cu_2S$	$Cd_{0.7}Zn_{0.3}S/Cu_2S$
OCV (volts)	0.51	0.55	0.6	0.62
SCC(mA/cm^2)	15.5	14	12.5	10
FF	0.6	0.59	0.6	0.58

The series resistances of the devices were measured using the flash lamp technique and were found to be comparable. The composition of the mixed crystal was verified from the band gap response[22].

Post barrier heat treatment of the junctions on mixed crystals reduced the SCC. In the device formed on $Cd_{0.8}Zn_{0.2}S$ the OCV increased from 0.6V to 0.62V while SCC deteriorated from 12 mA/cm^2 to 10 mA/cm^2 after heating at 200°C for 7 min. The spectral response of the device after this treatment is shown in Fig 6.9. The heat treatment enhanced the peak at 0.78 μm.

6.4.3 Photocapacitance Studies

Steady state photocapacitance curves obtained for devices formed identically on CdS and $Cd_{0.8}Zn_{0.2}S$ single crystals measured at L.N. and at room temperature are shown in Fig 6.10. At room temperature both devices showed a quenching of photocapacitance at a threshold of 0.75 eV which was

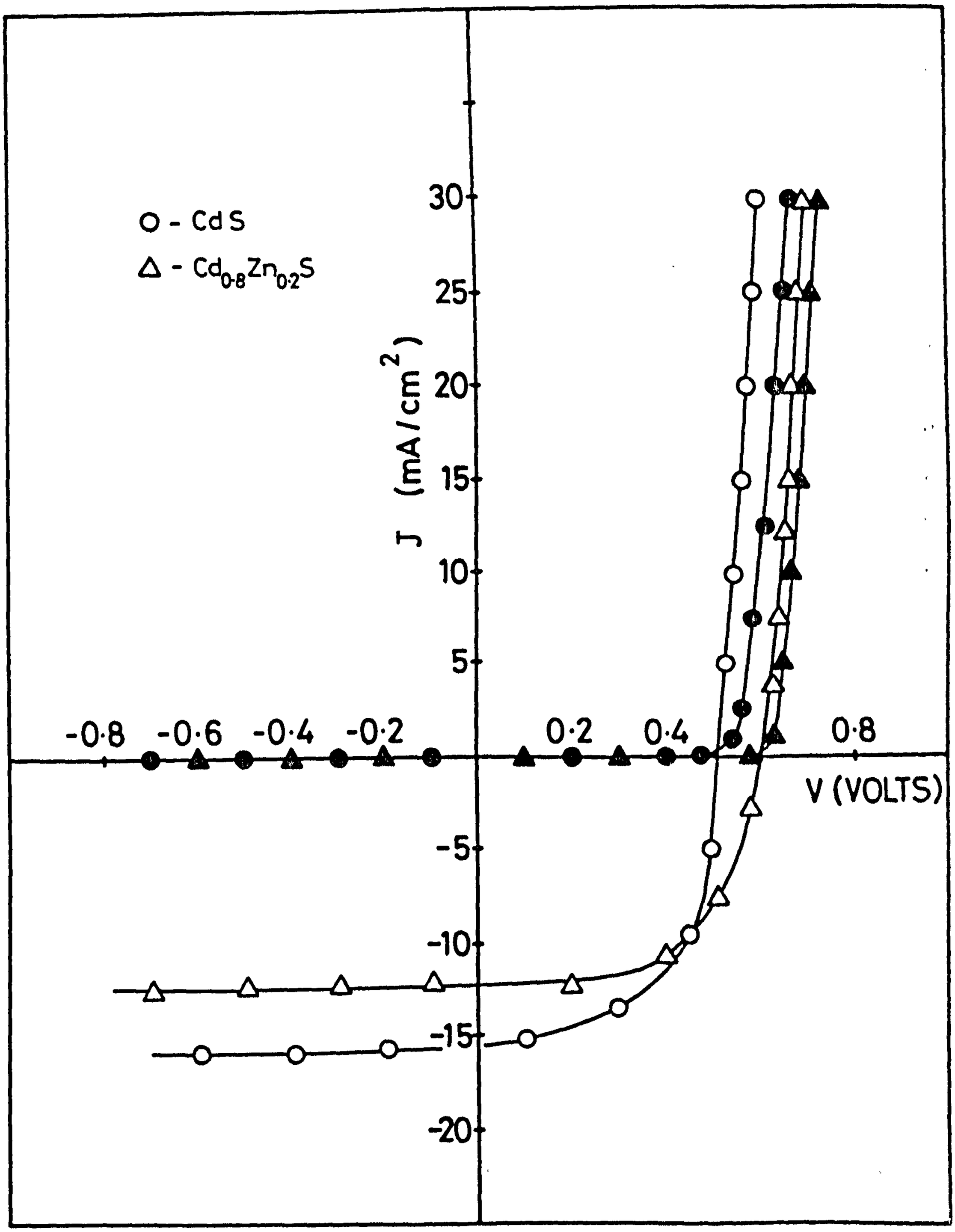


FIGURE 6.8: Current-voltage characteristics of heterojunctions formed on CdS and $Cd_{0.8}Zn_{0.2}S$ single crystal substrates.

Open symbols : light characteristics (under AM 1 illumination)

Closed symbols: dark characteristics.

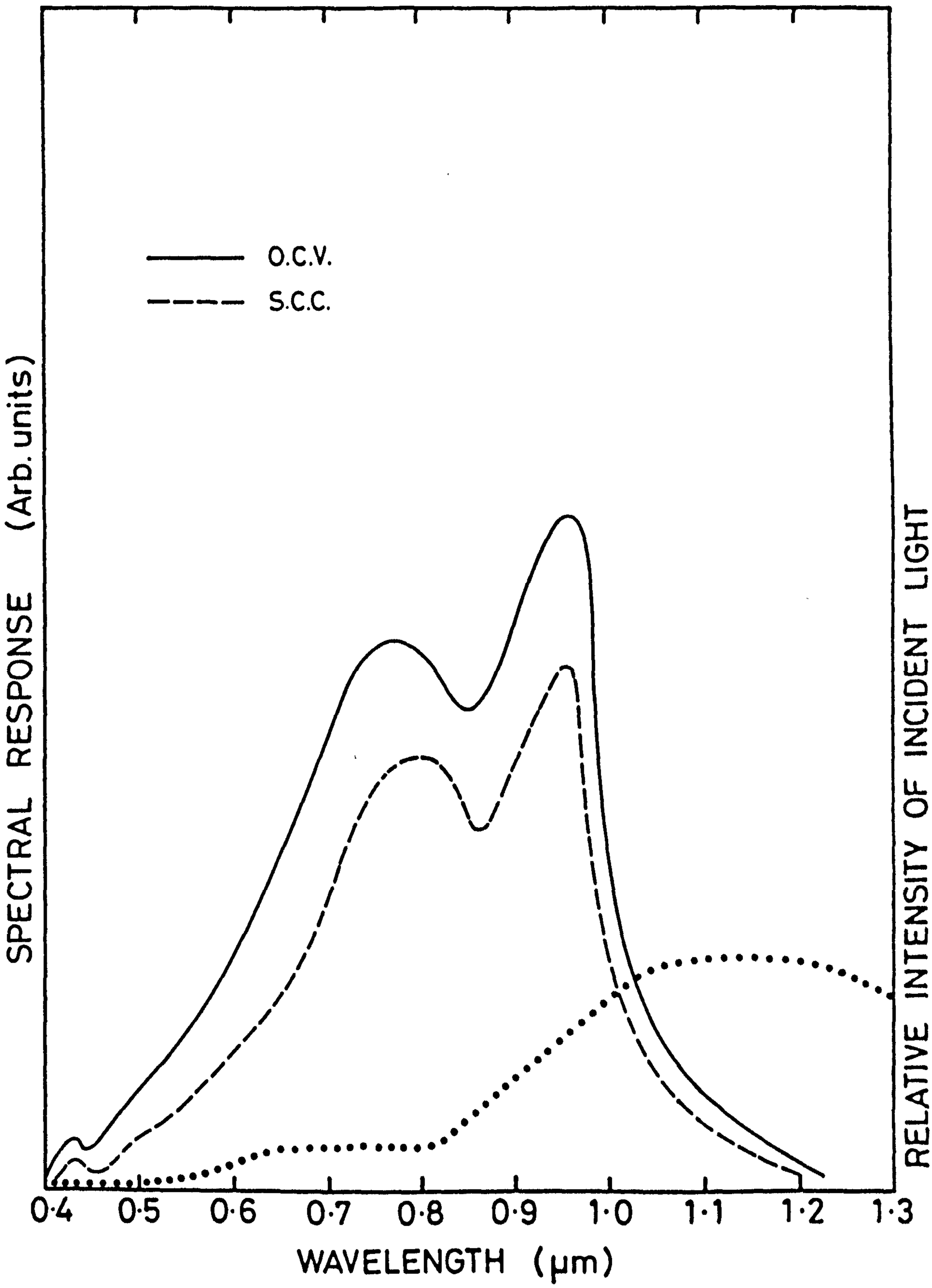


FIGURE 6.9: Spectral response of $Cd_{0.8}Zn_{0.2}S/Cu_xS$ device measured at 85 K after post barrier heat treatment.

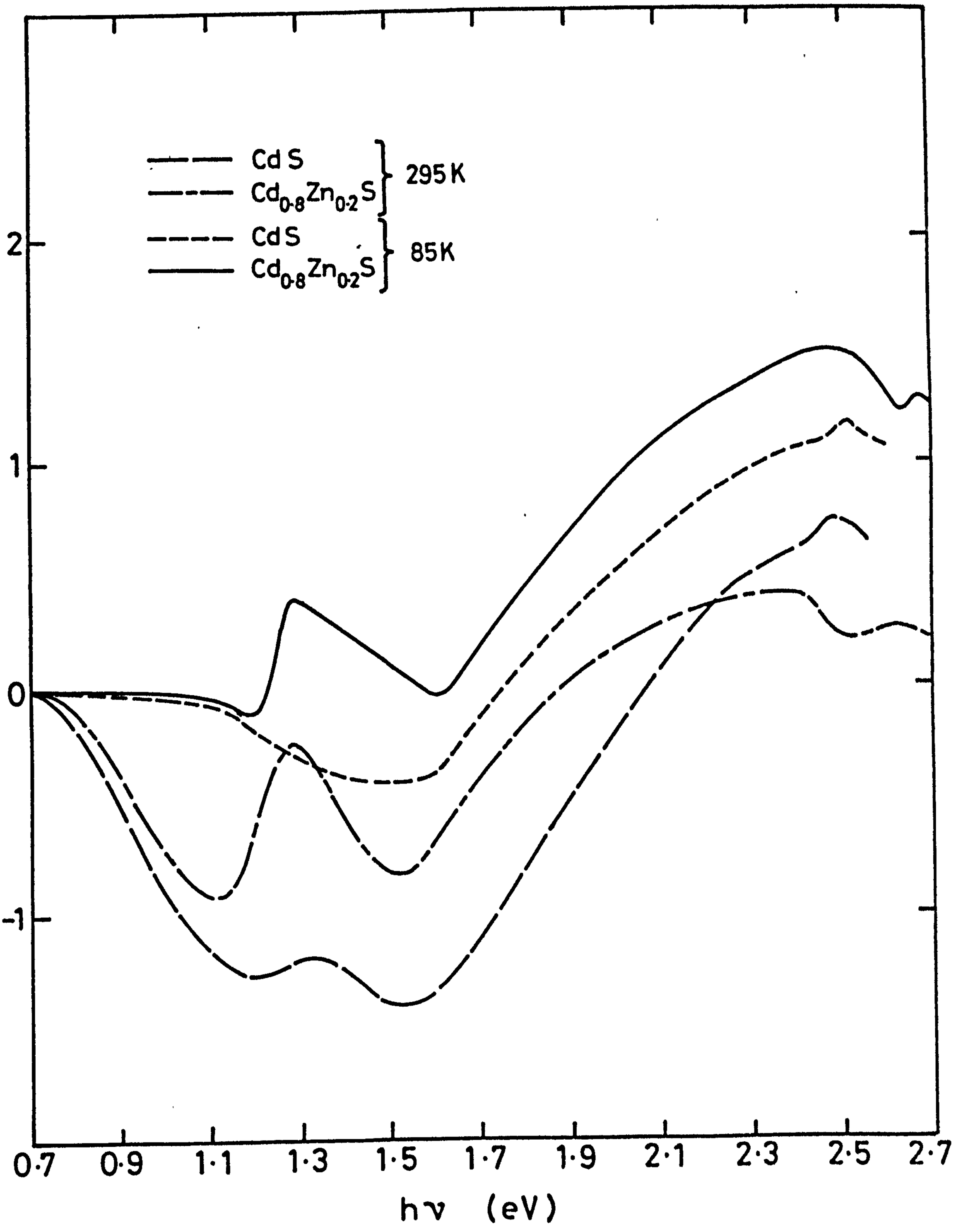


FIGURE 6.10: Photocapacitance spectra of heterojunctions formed on $Cd_{0.8}Zn_{0.2}S$ and CdS single crystal substrates.

not observed at 85K. At 295K this quenching extended to 1.15 eV, at which energy there was a significant rise in the photocapacitance for the device formed on $Cd_{0.8}Zn_{0.2}S$. Within this energy range, measurements made at 85K show that there is a threshold at 1.1 eV for a quenching process which can just be seen with the $Cd_{0.8}Zn_{0.2}S$ device, although it is very pronounced in the cell formed on CdS. The fall in the photocapacitance for the $Cd_{0.8}Zn_{0.2}S$ device was only just observable because of the abrupt enhancement at 1.22 eV. At energies above 1.3 eV a further quenching process was observed for both CdS and $Cd_{0.8}Zn_{0.2}S$ at 295K. This was more pronounced in the mixed crystal device. At 85K a similar quenching process was observed for the mixed crystal device, then the threshold was more precisely located at 1.27 eV. No such feature was observed at this energy for the CdS device when the temperature was reduced to 85K. For energies above about 1.6 eV the photocapacitance spectra of devices fabricated on both types of substrate at 85K and 295K reveal a pronounced enhancement which extends to an energy of about 2.3 eV for all cells formed on CdS, and to about 2.4 eV for devices based on mixed crystals. With the CdS cells increasing the energy beyond 2.3 eV gives rise to a small increase in photocapacitance. On the other hand a sharp fall was observed at 2.4 eV at 285K and 2.48 eV at 85K for the mixed crystal device.

The photocapacitance spectra can be explained by reference to Fig.6.11 where different trapping levels are shown in the depletion region. During the fabrication of heterojunctions on CdS it was demonstrated in Section 6.2 that some copper diffuses into the CdS and forms deep acceptors with hole ground and excited states lying 1.1 eV and 0.35 eV above the valence band. It has already been explained that the quenching of photocapacitance in CdS cells at 0.78 eV is related to the excitation of the holes from the deep acceptor ground state to excited state, from where the holes are thermally freed to the valence band. Since the photocapacitance spectrum of the device formed on $Cd_{1-y}Zn_yS$ also shows a quenching at 0.75 eV at R.T. and at 1.1 eV at

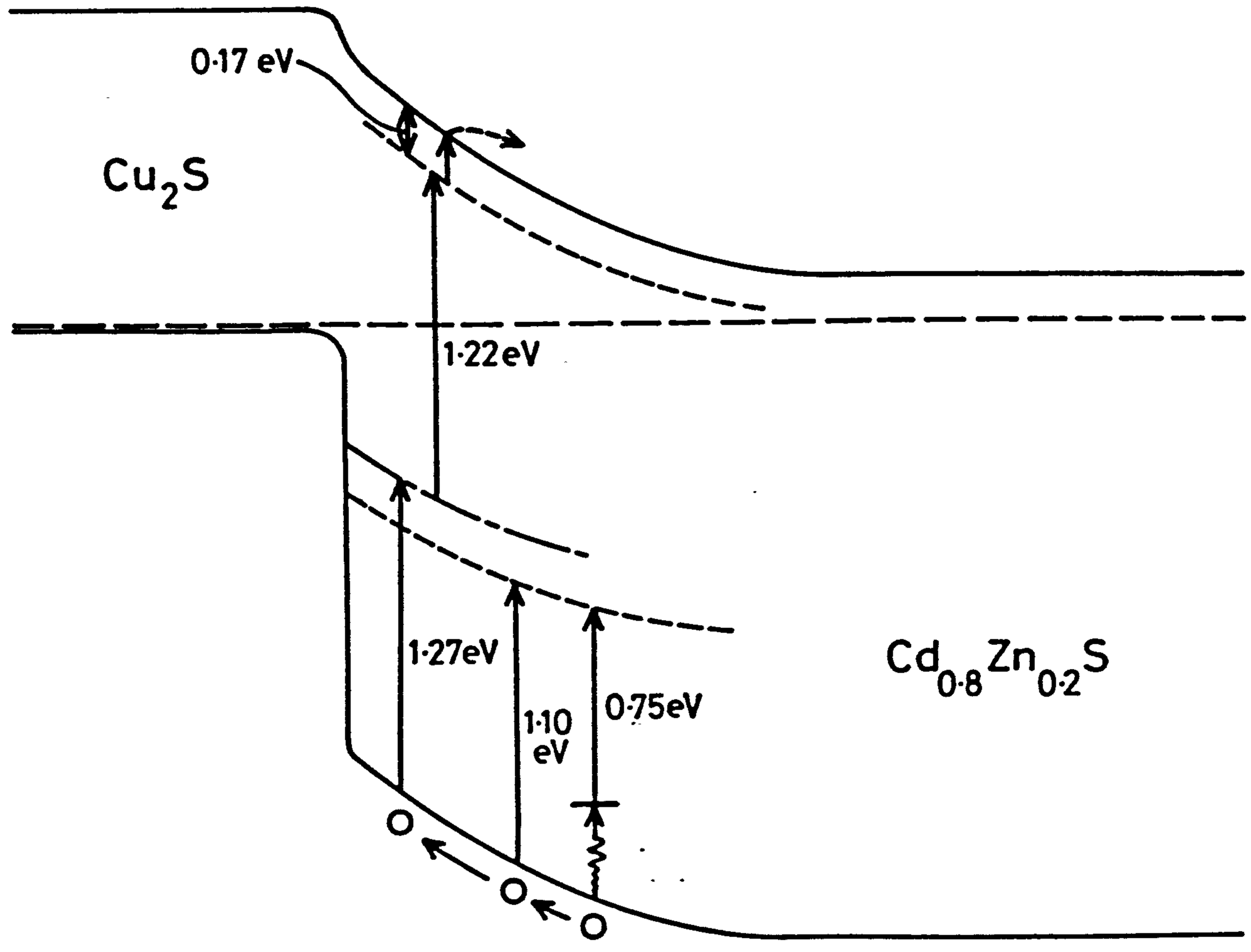


FIGURE 6.11: Energy band diagram of a $Cd_{0.8}Zn_{0.2}S/Cu_2S$ heterojunction at zero bias illustrating the different processes of quenching and enhancing the photocapacitance.

L.N. temperature, it can be inferred that identical copper acceptor levels were also formed by diffusion of copper. The enhancement and quenching of the photocapacitance at 1.22 eV and 1.27 eV at 85K for the $Cd_{1-y}Zn_yS$ device suggest the presence of a recombination centre with a level 1.27 eV above the valence band. With the incident energy of 1.22 eV the electrons are excited from this centre to the conduction band through a donor level lying 0.17 eV below the conduction band and this causes the enhancement in the photocapacitance. On illuminating the device with radiation with photon energy of 1.27 eV, electrons excited from the valence band are captured at this centre and a sharp fall in photocapacitance ensues. This feature was the most distinctive part in this photocapacitance spectra which was not observed in the curve for the device formed on CdS, although CdS cells heated in air did give a similar response where the quenching at 1.1 eV was followed by a rise and fall of the photocapacitance at 1.4 and 1.5 eV (Fig 6.1). This was explained in terms of the temporary arresting of the quenching via transitions to an acceptor state at the interface associated with oxygen adsorption and lying 0.2 eV below the conduction band. However since the mixed crystal devices were heated in argon, the rise and fall of photo-capacitance at 1.22 eV and 1.27 eV must be attributed to a different trap.

The rise at 1.6 eV corresponds to the excitation of electrons from the deep copper acceptor states (not all of them are filled) to the conduction band. This was a common feature in devices formed on both CdS and $Cd_{0.8}Zn_{0.2}S$. A sharp fall in the photocapacitance curve of the $Cd_{0.8}Zn_{0.2}S$ cell at 2.48 eV close to the band gap reveals a donor level. The negative threshold suggests a process of capturing electrons excited from the valence band. In fact this feature was also observed in the photocapacitance of a Schottky device on $Cd_{0.8}Zn_{0.2}S$ (Fig 6.12). From this curve it is evident that two negative thresholds exist at 1.05 eV and 2.48 eV, while a positive threshold occurs at 1.58 eV. The negative threshold at 2.48 eV corresponds to the donor level

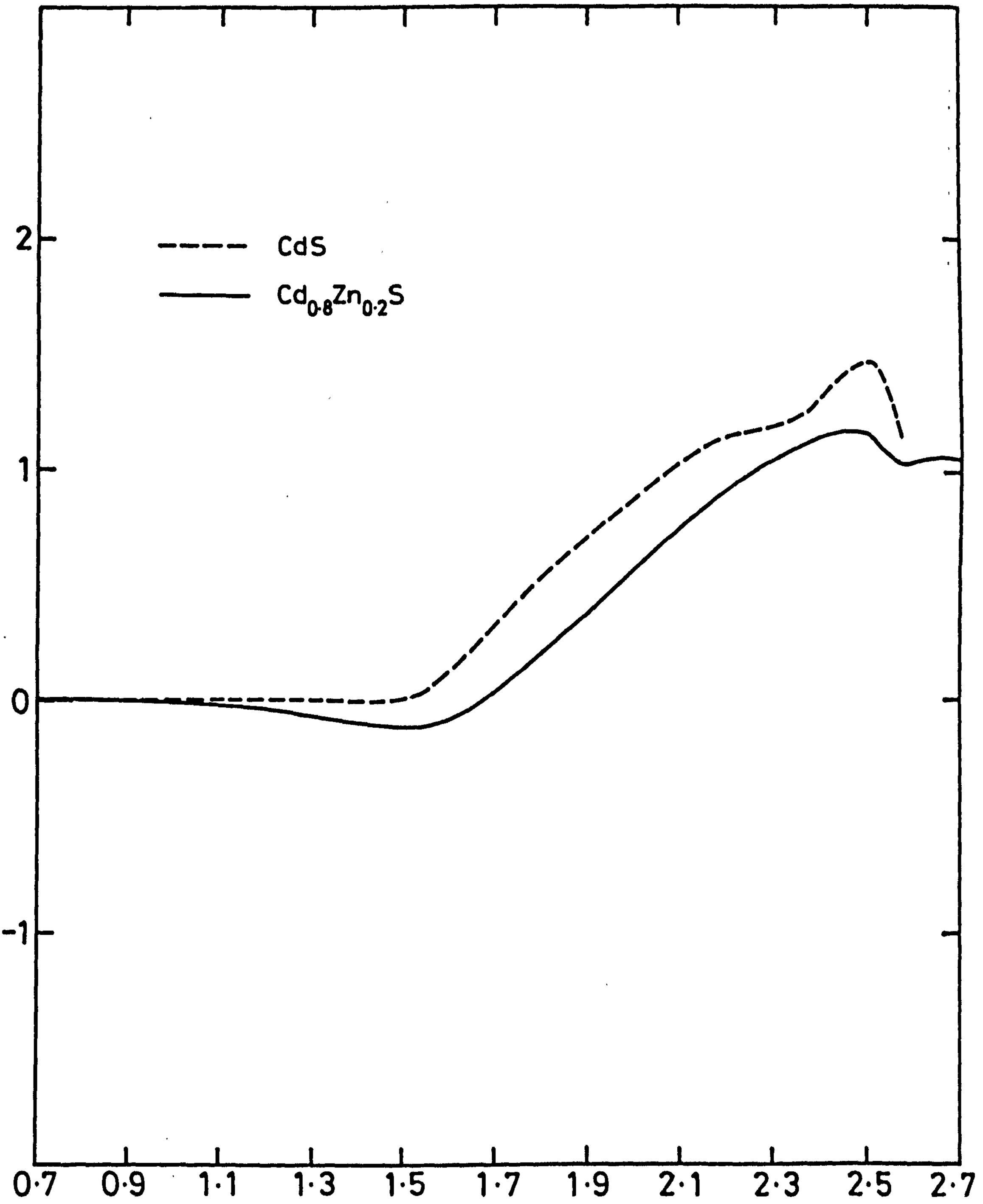


FIGURE 6.12: Photocapacitance spectra (measured at 85 K) of Schottky devices on CdS and $Cd_{0.8}Zn_{0.2}S$ single crystal substrates.

just discussed, which lies .17 eV below the conduction band. No such feature was observed in the photocapacitance spectra for Schottky devices formed on CdS. The rise at 1.58 eV is due to excitation of electrons from a level ∿ 1 eV above the valence band which might be due to cadmium vacancies since no copper was involved in the Schottky device. The negative threshold at 1.0 eV corresponds to the filling of the same level from the valance band. This was not observed in the CdS Schottky which suggests a difference in the occupation and density of this level compared with $Cd_{1-y}Zn_yS$.

Although the photocapacitance spectra for the mixed crystal device could be explained by the model suggested in Fig 6.11, a few anomalies are associated with the explanations given. In heterojunction devices, if the trap level is lying 1.27 eV above the valence band, an emptying process should have taken place with photons of energy 1.38 eV which would have resulted in the excitation of photocapacitance. Instead the excitation takes place at 1.22 eV. In the Schottky device the process of quenching and excitation of photocapacitance take place at 1.0 eV and 1.58 eV. The sum of these two energies (2.58 eV) should be at least equal to the band gap but it seems slightly too low. These two features show that the excitation process from the trap level to the conduction band is not behaving as it should for a direct band gap material. It is suggested that the inclusion of zinc in the CdS lattice might have caused some local inhomogeneity leading to band tailing similar to that in amorphous material so that excitation in these tail states would occur at a lower value than expected.

6.5 DISCUSSION

The model of the potential energy diagram of the CdS-Cu_2S heterojunction most frequently employed, is basically that developed by Shiozawa et al[23], as modified by Fahrenbruch and Bube[3] and others[24,25]. The dominant feature of this scheme is that there is a discontinuous notch of about 0.35 eV at the junction between the conduction bands of the Cu_2S and

the CdS. When cells are prepared by the more commonly employed wet plating method[23], it is usually necessary to administer a short bake at $\sim$ 200°C in air, before optimum efficiency is obtained. It is now agreed that one function of the bake is to promote the diffusion of Cu^+ ions into the n-type CdS at the junction, forming a narrow photoconducting i-layer there.

The dry barrier method of preparing heterojunction cells was first proposed by Te Velde[26,27]. Technologically it is most important for use with very thin base layers of CdS. However the detailed nature of the potential barrier produced in this way has received very little attention in the literature. Baking at low temperature is again a feature of the preparation of efficient devices, but Te Velde[26] himself was of the opinion that little copper diffused into the CdS, and no photoconducting layer was formed. He suggested that the prime function of the bake was to induce the adsorption of oxygen at the interface, which would introduce acceptor states, and increase the band bending in the CdS. The effect of this would be substantially to reduce the size of the notch at the junction.

The results described here demonstrate conclusively that copper does diffuse into the CdS when the heterojunction is formed by the dry barrier process. The thresholds for infrared quenching (Fig 6.1) show that the binding energies of the ground and excited hole states of the copper acceptor are at 1.1 and 0.35 eV above the valence band respectively. This is in excellent agreement with the conclusion of Grimmeiss et al[28] and in reasonable agreement with the results of Lindquist and Bube[2].

The infrared quenching of photocapacitance also exhibited additional features with those heterojunctions which had been heated in air following the first stage of preparation. A possible interpretation of the small maximum observed in the middle of the large quenching dip (Fig 6.1) is that it is associated with the presence of acceptor levels due to adsorbed oxygen at the interface. Transitions from the electron filled copper levels, 1.1 eV

above the valence band to the oxygen acceptor at the interface 0.2 eV below the conduction band of the CdS would then lead to a maximum in the photo-capacitance similar to that observed. Such a suggestion would provide excellent support for Te Velde's ideas. Earlier work by Robertson and Woods[29] also led to the conclusion that oxygen was adsorbed at the inter-face in wet plated cells which had been given the short sensitising air bake.

It is quite clear from this study that energy states other than those associated with copper acceptors and shallow donors are present in the depletion region. The justification for this statement in the observation of dips and maxima in the copper diffusion profiles (Fig 6.4). Such effects are very reminiscent of features of the 'push out' effect in diffused silicon transistors when the diffusion of acceptors (Ga) and donors (P) is carried out sequentially[30]. During the second diffusion of phosphorus, the leading edge of the gallium profile, well ahead of phosphorus, is pushed further out from the interface. This is due to enhanced diffusivity of the gallium. At the same time the gallium profile develops a minimum very similar to that depicted in Fig 6.4 for the device heated in air. This suggests that more than one species is diffusing in the CdS during the post preparative heat treatments.

It is interesting to note that the J-V characteristics of the devices heated in air and in argon were also found to be different (see Section 5.4.1). In particular the devices heated in air had poor fill factors compared to those heated in argon. The detailed shapes of the current voltage characteristics depend on a large number of parameters, see for example Boer[31] who has generated numerically a number of J-V characteristics for various different values of the parameters in his model. He obtained curves very similar in shape to those measured in our studies for the cells heated in air. In those particular curves Boer had assumed a model containing two dominant electron traps in the depletion region of the CdS with ionization energies of 0.22 and

0.65 eV. Such traps may be enhanced by baking in air. In contrast, our experimental cells heated in argon have harder characteristics which are responsible for the improved fill factor. The excellent shape of these J-V curves could be associated with a reduced concentration of electron traps, or with a reduced rate of recombination through the interface states[31].

The effect of heat treatment on the device parameters has been discussed by Hseih[32] in terms of the copper diffusion by considering the solution of the one dimensional Poisson equation with appropriate boundary conditions, and a diffusion model with a Gaussian profile for the Cu acceptor concentration in CdS. However, this model was based on assumed values of the parameters which related the fraction of copper acceptor diffused in the n-CdS region and the fill factor of the device after heat treatment. In the actual experiments carried out on heat treated CdS/Cu_xS heterojunctions Hmurick et al[33] observed certain anomalies in the linearity of C^{-2} -V plots which they attributed to deep traps formed during the heat treatment. However, with their measurement technique the spatial distribution of the deep traps could not be determined. In this connection our results on the profile of the copper levels are quite significant. In all the air heated devices when a dip in the copper profile was observed, an additional feature in the photo-capacitance spectra also appeared which was attributed to acceptor-like states formed at the interface due to adsorption of oxygen[34]. It is suggested that because of the presence of this additional trap and a different spatial distribution of copper levels in the CdS in air heated device, the J-V characteristics are affected in such a way that they give rise to shoulders at $\sim$ $\pm$ 0.4V in forward and reverse bias which results in a reduced fill factor. In contrast the spatial distribution of the copper levels in the cells heated in argon had a pronounced maximum and no additional feature

appeared in the photocapacitance spectrum except that due to acceptor states formed due to copper diffusion. Moreover heat treatment in argon led to an excellent J-V characteristic. These facts suggest that the effects occurring at the interface depend upon the ambient during the heat treatment, which in turn affects the device characteristic.

Interface effects and their relationship with device parameters are also significant in the heterojunctions formed on $Cd_{1-y}Zn_yS$. The OCV under AM 1 illumination increased from 0.51 to 0.62V with increasing zinc content ($0 < y < 0.3$) but the SCC decreased from 15 mA/cm^2 to 10 mA/cm^2. The increased value of OCV has been reported by other workers who have attributed it to an increase in the barrier height[11,18,35]. It has been suggested that the incorporation of zinc in CdS minimises the difference in the electron affinities[35-38] and reduces the lattice mismatch between CdS and Cu_2S. With a better match of electron affinities the height of the conduction band step (0.2 eV for CdS and Cu_2S) decreases so that the barrier height increases[38].

Since $V_{oc} = \frac{kT}{q} \text{ Ln } (\frac{J_L}{J_0} + 1)$, all the parameters which lower the value of J_o should make a positive contribution towards the open circuit voltage. With the present model where interfacial recombination processes are considered as the dominating feature in CdS/Cu_xS heterojunctions[39], $J_o = q N_c S_I \exp(-q\phi/kT)$. Here the interface recombination velocity $S_I = v_{th} \sigma_n N_I$ depends upon the electron capture cross section (σ_n) and interface state density (N_I). The better lattice match should reduce N_I which lowers J_o and hence help to increase the OCV. The upper theoretical limit of the OCV has been calculated to be 0.85 V for $Cd_{1-y}Zn_yS$ heterojunctions assuming $N_1 = 0$[35].

With the decrease in the density of interface states, the interfacial collection factor[25] ($ICF = \frac{\mu F}{S_I + \mu F}$) should also increase, which implies that a larger photo-current density should also result. The mobility and field

at the interface are the other factors which would influence ICF. There are not many reports available on the mobility of the mixed crystals. Romeo et al[40] report Hall mobilities of the $Cd_{1-y}Zn_yS$ film parallel to the substrate varying from 100 to 20 $cm^2 V^{-1} s^{-1}$ as y goes from 0 to 0.3. Sakurai et al[41] found values of 60 $cm^2 V^{-1} s^{-1}$, while Kwok et al[42] have reported decreasing values of Hall mobility with increase in zinc content. As far as the electric field is concerned the dark capacitance of a hetero-junction formed on $Cd_{1-y}Zn_yS$ was invariably found to be larger compared to devices formed on CdS, which suggestsa narrower depletion region and higher values of electric field. Although no attempt has been made to determine the value of the ICF completely, the increased magnitude of the electric field should contribute to a larger SCC unless $S_1 \ll \mu F$. In contrast the present study has shown that the SCC was much lower in the $Cd_{1-y}Zn_yS$ devices. This lowering of the SCC in the $Cd_{1-y}Zn_yS$ heterojunction has also been observed by other workers[11-20,35-36] who offered a variety of explanations. With wet plated cells the lowering of the current density has been attributed to the difficulty in forming a layer of the desired phase (chalcocite $Cu_{2.0}S$)[16,17,35]. The present study has shown that a predominantly chalcocite layer is formed on $Cd_{1-y}Zn_yS$ when the dry barrier process is used as evidenced by the 0.96 μm peak in the spectral response[43,44]. Moreover the spectral response measured at L.N. temperature gives a better indication of the phase. From curves (Figs 6.6, 6.7) measured at L.N. temperature, it was quite obvious that the devices formed by the dry barrier process on $Cd_{0.8}Zn_{0.2}S$ and $Cd_{0.7}Zn_{0.3}S$ substrates had a major peak associated with chalcocite, whilewet plated devices displayed an additional peak at 0.78 μm indicating the presence of djurleito. Other workers have also found that the dry barrier process produces a chalcocite layer on $Cd_{1-y}Zn_yS$[15,19]. It was quite noticeable that the reaction in $Cd_{1-y}Zn_yS$ proceeded more slowly than on CdS. However a prolonged reaction time (6 min) gave a djurleite response, which can be attributed to the process

of inter-diffusion of Cu in the $Cd_{1-y}Zn_yS$ and Cd and Zn in the Cu_xS layer. The diffusion of zinc in the Cu_xS layers in the cells prepared by wet plating was observed by Burton et al[45] who found that after heat treatment it increased substantially. Though no such measurements were made during this study, it seems that this cross diffusion effect is much less during the initial stages of the dry barrier reaction. Since chalcocite is readily produced by the dry barrier process on $Cd_{1-y}Zn_yS$ some other explanation for the lowering of SCC must be sought. One possibility[34] is that a layer rich in zinc is accumulated at the interface which results in the formation of a potential spike[38,46]. This region of a given grain could be effectively 'dead'. As the zinc content increases the fraction of this accumulated region increases due to enhanced accumulation of zinc under the interface and this has been assumed to be a major factor for the decrease in the SCC[35]. However, these conclusions were drawn from a study of wet plated cells where single phase layers of the copper sulphide were not obtained.

An additional mechanism has been proposed by Boer[47] in which it is assumed that a spike exists at the interface which is essentially transparent to electron flow across the interface. As the lattice mismatch improves the amplitude of the spike decreases and its width increases. This reduces the electron tunnelling probability and the SCC decreases. However, this model is not consistent with current ideas where a step is thought to occur at the CdS/Cu_2S junction. Another possibility is that there will be high series resistance[20] due to higher resistivity of $Cd_{1-y}Zn_yS$, and the accumulated layer of zinc at the interface. The resistivity of the substrate depends on the growth conditions[42]. In the experiments carried out here on $Cd_{1-y}Zn_yS$ devices with a wide range of composition, it was found that the series resistances were of similar magnitude and practically no difference in FF was detected, although the SCC decreased.

Our measurements of steady state photocapacitance suggest a new possibility. It is suggested that the positive threshold at 1.22 eV in the photocapacitance spectrum (Fig 6.10) for the device formed on $Cd_{0.8}Zn_{0.2}S$ is associated with a recombination centre lying 1.27 eV above the valence band. The room temperature measurements show that although copper does diffuse into the $Cd_{1-y}Zn_yS$ the change in photocapacitance in this region of the spectrum is dominated by this new centre. It is thought[35] that a layer of zinc accumulates at the interface during device fabrication and it seems possible that during the heat treatment cation vacancy complexes develop in the zinc rich region to form a new recombination centre. An additional donor level is observed at 0.17 eV below the conduction band in both the Schottky and heterojunction devices formed on $Cd_{0.8}Zn_{0.2}S$. This donor may be the corresponding anion defect in the zinc rich region. It is suggested therefore that the major cause in the reduction in the current density in the devices formed in $Cd_{1-y}Zn_yS$ is due to this new recombination centre which is formed in the depletion region and lies 1.27 eV above the valence band. No such centre was observed in the devices formed on CdS.

Following post barrier heat treatment the device spectra indicated an increasing djurleite content. The reduction in the SCC with post preparative heat treatment can be attributed to the deterioration in the stoichiometry of the Cu_2S by the process of inter-diffusion of Cu in $Cd_{1-y}Zn_yS$ and (Cd,Zn) in Cu_2S[45]. The formation of deep acceptor states due to copper diffusion in the $Cd_{1-y}Zn_yS$ is obvious from the photocapacitance spectra, which demonstrates that copper forms deep acceptor states in $Cd_{1-y}Zn_yS$ in the same way as in CdS with hole ground and excited states 1.1 eV and 0.35 eV above the valence band. In the absence of copper, acceptor centres, formed due to cadmium vacancies,lie at $\sim$ 1.0 eV above the valence band which was revealed from the photocapacitance spectra of the CdS and $Cd_{1-y}Zn_yS$ Schottky devices. These defects are known to exist in CdS and depend on the growth condition and added impurities[48,49,50].

6.6 CONCLUSION

This study has revealed that device parameters in cells formed on CdS and $Cd_{1-y}Zn_yS$ are strongly affected by the processes which occur at the interface during the heat treatment. The photocapacitance studies show that copper diffuses into the CdS and $Cd_{1-y}Zn_yS$ and produces a deep acceptor, with hole ground and excited state 1.1 and 0.35 eV above the valence band. Evidence was obtained which suggests that heating in air leads to acceptor-like states at the interface,0.2 eV below the conduction band. The measured copper profile in the CdS was anomalous, and indicates that more than one diffusing species was active. In the cells formed on $Cd_{1-y}Zn_yS$ by the dry barrier process, the dominant phase of the Cu_xS layer was chalcocite. Although the OCV increased with the incorporation of zinc, the SCC decreased. It is suggested that this is due to the presence of a recombination centre 1.27 eV above the valence band.

REFERENCES TO CHAPTER 6

1. W.D. Gill and R.H.Bube: J.Appl.Phys. 41 (1970), p.3731.

2. P.F.Lindquist and R.H.Bube: J.Appl.Phys. 43 (1972), p.2839.

3. A.L.Fahrenbruch and R.H.Bube: J.Appl.Phys. 45 (1974), p.2134.

4. W.G.Hainesand R.H.Bube: IEEE.Trans.Electron Devices ED-27 (1980), p.2133.

5. W.J.Manthey, Annual Report XS-9-3309-1, Institute of Energy Conversion, Univ.of Delaware, Dec.1980,p.63.

6. P.De Visschere, H.Pauwels, L.Vandendriessche.M.Burgelman and A.De Vos in Proc.Fifth E.C.Photovoltaic Solar Energy Conference, (D.Reidel Publ.Co.)Kavouri (Athens), Greece, 17-21 October1983,p.878.

7. L.C.Burton and H.Windawi, J.Appl.Phys. 47 (1976) p.4621.

8. L.Hmurick,L.Allen and R.A.Serway: J.Appl.Phys. 53 (1982) p.9063.

9. L.D.Partain, P.S.McLeod, J.A.Duisman, T.M.Peterson, D.E.Sawyer and C.S.Dean, J.Appl.Phys. 54, (1983), p.6708.

10. T.Suda and R.H.Bube: J.Appl.Phys.52, (1981), p.6218.

11. A.M.Barnett and A.Rothwarf: IEEE Trans.Electron Devices ED-27, 4 (1980), p.615.

12. W.Palz, J.Besson, J.N.Duy and J.Vedel: Proc.10th IEEE.Photovoltaic Specialists Conf. Palo Alto,C.A, (1973), p.69.

13. R.B.Hall, R.W.Birkmire, J.E.Phillips and J.D.Meakin, Appl.Phys.Letts 38, (1981), p.925.

14. L.C.Burton: Proc.South East.Conf.80, Nashville,April 1980, New York, (1980), p.116.

15. S.Martinuzzi, F.Z.Nataren, D.Vassilevski, B.Bouchikhi, M.Cadene, M.Moutaki and M.Rolland: Proc.3rd E.C.Photovoltaic Solar Energy Conf.Cannes, (1980) (Reidel,Dordrecht 1981), p.782.

16. S.Oktik, G.J.Russell and J.Woods, Solar Cells 5, (1982), p.231.

17. S.Oktik, G.J.Russell and J.Woods, J.Cryst.Growth 59, (1982), p.414.

18. S.R.Das, A.Banerjee and K.L.Chopra: Solid State Electronics 22 (1979), p.533.

19. M.S.Tomar and F.J.Garcia: Jap.J.Appl.Phys. 19 (1980), p.567.

20. V.P.Singh and J.F.Jordan: IEEE Electron.Devices Letters, Vol.EDL-2 6 (1981), p.137.

21. T.Suda, K.Matsuzaki and S.Kurita: J.Appl.Phys. 5, (1979), p.3638.

22. V.P.Singh and S.Singh, Czech.J.Phys. B. 26 (1976), p.1163.

23. L.R.Shiozawa, G.A.Sullivan, F.Augustine, J.M.Smith, and W.Cook: Final Tech.Rept.AF 33(615)-5224, Project No.7885, (1969), ARL 69-0155.

24. A.Rothwarf and K.W.Boer: Prog.Solid State Chem.10 (1972) p.71.

25. A.Rothwarf, Solar Cells 2 (1980), p.115.

26. T.S. Te Velde, Solid State Electronics 16, (1973), p.1305.

27. T.S. Te Velde, Energy Conversion, 15, (1975), p.111.

28. H.G.Grimmeiss, N.Kullendorff and R.Brosce, J.Appl.Phys.52, (1981),p.3405.

29. M.J.Robertson and J.Woods, Proc.2nd E.C.Photovoltaic Solar Energy Conf. Berlin (Dordrecht,Reidel) (1979), p.909.

30. A.F.W.Willoughby: J.Phys.D.Appl.Phys. 10, (1977), p.455.

31. K.W.Boer: Phys.Stat.Solidi a 66, (1981), p.11.

32. H.C.Hseih: J.Appl.Phys. 33, (1982), p.1727.

33. L.H.murick, L.Ketelsen,R .A.Serway: J.Appl.Phys. 53, (1982), p.3839.

34. P.C.Pande, G.J.Russell and J.Woods; J.Phys.D.Appl.Phys. 16, (1983),p2307.

35. L.C.Burton: Solar Cells, 1 (1979/80)) p.159.

36. L.C.Burton and T.L.Hench: Appl.Phys.Letters 9 (1976),p.611.

37. S.Martinuzzi,J.Oualid,D.Sarti and J.Gervais: Thin Solid Films 52 (1978), p.211.

38. L.C.Burton: Appl.Phys.Letters 35, (1979), p.780.

39. A.Rothwarf: Proc.Intern.Workshop on CdS Solar Cells and other Abrupt Heterojunctions, Univ.of Delaware, Eds.K.W.Boer and J.Meakin,(1976) p.151.

40. N.Romeo, G.Sberveglieri and L.Tarricone; Appl.Phys.Lett.32, (1978)p.807.

41. Y.Sakurai, Y.Kokubun, H.Watanabe and M.Wada: Jap.J.Appl.Phys.16 (1977), p.2115.

42. H.H.L.Kwok, M.Y.Leung and Y.W.Lam : J. Crystal Growth 59, (1982), p.421.

43. B.G.Caswell, G.J.Russell and J.Woods: J.Phys.D.Appl.Phys.10(1977)p.1345.

44. P.C.Pande, G.J.Russell and J.Woods: Proc.5th E.E.C.Photovoltaic Solar Energy Conference, Athens, Greece, (1983). p.171.

45. L.C.Burton, P.N.Uppal, D.W.Dwight: J.Appl.Phys. 53, (1982), p.1538.

46. W.B.Hsu and L.C.Burton: J.Electronic Materials 1C, (1981), p.703.

47. K.W.Boer: J.Appl.Phys. 50 (1979), p.5356.

48. R.H.Bube: Electronic Properties of CrystallineSolids, An Introdction to Fundamentals, Academic Press, New York (1974).

49. I.B.Ermolovita, V.V.Gorbunov, and I.O.Konozenko: Sov.Phys.Semi.Cond. 11 (1971). p.1061.

50. M.Hussein, G.Lleti, G.Sagnes, G.Bastide and M. Rouzeyre, J.Appl.Phys. 52 (1981) p.261.

CHAPTER 7

ASSESSMENT OF ELECTROPHORETICALLY DEPOSITED THIN FILMS OF CdS

7.1 INTRODUCTION

The study of the dry barrier process for fabricating heterojunctions on single crystal substrates has been extended to films of CdS deposited by electrophoresis. In general these films are very thin (1-2 μm), exhibit the sphalerite structure, and have a resistivity $\gtrsim 10^6$ Ωcm. To improve their suitability for use as substrates for photovoltaic devices, they have been given different annealing treatments in the presence of halide and non-halide fluxes. The structural effects of annealing in different ambients and in the presence of different dopants were investigated by RHEED and in the SEM. The resistivities of the films were measured at different stages of the annealing treatments, and subsequently current voltage, capacitance-voltage and photocapacitance studies were made on Schottky devices formed on these films. Heterojunctions were prepared by the dry barrier process and the device characteristics recorded. In addition, thermal annealing experiments were performed on thicker films ($\tilde{\sim}$ 10μm) which were obtained by incorporating polyvinyl pyrollidine as a binder in the plating bath during electrophoresis. Improved photovoltaic devices were fabricated on these thicker films.

7.2 AS-PREPARED FILMS

The films were deposited at Thorn EMI, Hayes, London, following the method described by Williams et al[1,2]. The solution was prepared with a particle size of $\sim$ 100 Å, by bubbling H_2S through an aqueous solution

of cadmium acetate. Immediately before electrophoresis, the solution was diluted with methanol and its pH adjusted to between 5 and 6 by adding ammonia. Anodic deposition was carried out using a voltage of 200 V with an electrode spacing of 6 cm. The current density was some 2 mA cm^{-2}. Uniform films free of pinholes were produced provided they did not exceed 2 μm in thickness. The RHEED pattern from an as-received film is shown in Fig.7.1. The interplanar spacings calculated from this are given in Table 7.1 where they are compared with the values from the ASTM index for both cubic and hexagonal CdS. The observed intensities of the diffraction rings suggest that the as-made film consists predominantly of sphalerite cubic phase CdS. The three bright rings in Fig.7.1 correspond to the (111), (220) and (311) reflections from cubic CdS and are indexed accordingly. This cubic phase must be transformed to hexagonal to ensure that the chalcocite phase of Cu_xS is produced by the chemical displacement reaction employed in the fabrication of the heterojunction[3]. In addition these films also had a high resistivity (> 10^6 Ωcm) which was estimated by measuring the resistance between indium dots evaporated on to the films and the tin oxide back contact. Clearly the structural and electrical properties are unfavourable for use in fabricating efficient photovoltaic cells.

Similar observations of the structure of electrophoretically and chemically deposited CdS films have also been reported by other workers[4,5,6]. At this point it is worth mentioning that the crystalline phase of the CdS particles depends strongly on the preparative conditions. For example, it has been shown[7,8] that in the precipitation of CdS by chemical means, the phase of the CdS, which is formed, is dependent on the particular salts of Cd used in the process.

In films put down by thermal evaporation[9] or spray pyrolysis[10,11] the substrate temperature affects the phase and orientation of the CdS. With this in mind, a few attempts were made to increase the substrate temperature

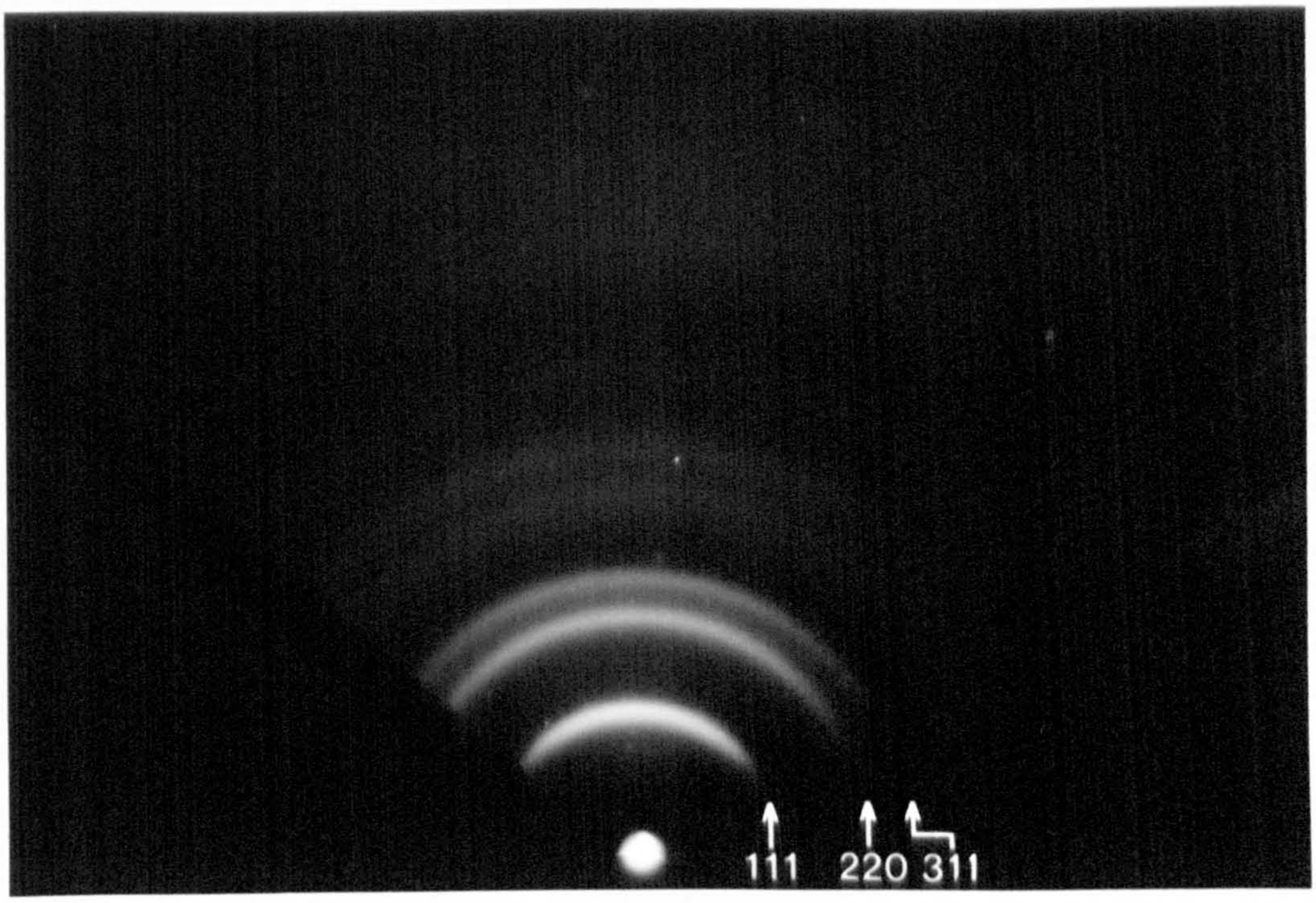


FIGURE 7.1: RHEED pattern from an as-made electrophoretically deposited film.

Ring	Measured Radius (cm)	Estimated Intensity	Measured d-spacing Å	Cubic CdS			hex CdS		
				d-spacing Å	Relative Intensity %	(hkl)	d-spacing Å	Relative Intensity %	(hkl)
R_1	1.7	vs	3.24	3.36	100	(111)	3.357	59	(002)
R_2	2.25	w	2.45				2.45	25	(102)
R_3	2.75	vs	2.00	2.058	80	(220)	2.068	57	(110)
R_4	2.95	w	1.87				1.898	42	(103)
R_5	3.2	vs	1.73	1.753	60	(311)	1.761	45	(112)
R_6	3.55	w	1.55				1.581	7	(202)
R_7	3.8	s	1.45	1.453	20	(400)			
R_8	4.0	s	1.38				1.398	15	(203)
R_9	4.15	vs	1.33	1.337	30	(331)	1.327	11	(211)
R_{10}	4.4	w	1.25				1.257	11	(105)
R_{11}	4.65	vs	1.19	1.186	30	(422)			
R_{12}	4.8	m	1.15				1.158	12	(213)
R_{13}	4.95	vs	1.11	1.12	30	(333)			
R_{14}	5.35	w	1.03	1.028	5	(440)			
R_{15}	5.65	vs	0.976	0.985	20	(531)			

ASTM DATA

TABLE 7.1: Indexing of RHEED Pattern from Unannealed Electrophoretic CdS

during electrophoresis but no advantage was obtained. This is probably because the temperature range suitable for deposition was only 50-70°C. Increasing the substrate temperature above 70°C increased the temperature of the solution and this led to several depositional difficulties. Changing the cadmium salts used gave no advantage although the presence of $CdCl_2$ in the solution did promote some hexagonal content in the films. However, it was then difficult to deposit uniform layers. Consequently it was decided to deposit cubic films and convert them to the hexagonal phase later.

7.3 THERMAL HEATING

The heat treatments were carried out in an open ended horizontal tubular electric furnace with the substrate carrying the electrophoretically deposited films either(1) supported in a silica boat with the surfaces of the film exposed directly to the furnace ambient, or (2) encapsulated in a silica ampoule containing materials chosen to provide a different controlled atmosphere during the heat treatment. In this series of annealing trials, a flow of argon (20 ml/min) was passed continuously through the furnace which was maintained at temperatures from 300 to 700°C. The samples were preheated for about 10 mins just inside the end of the furnace tube before being subjected to the full heat treatment. They were similarly cooled slowly afterwards.

7.3.1 Structural Aspects

The effects on the crystal structure of the various heat treatments are summarized in Fig.7.2 where microdensitometer traces of the reflection electron diffraction patterns obtained from CdS films annealed in argon at three different temperatures are shown. The peaks have been indexed from measurements of the diffraction patterns, and the (hkl) values are shown separately for the sphalerite and wurtzite phases on the diagram. The most important of the wurtzite reflections are (102) and (103) because unlike the

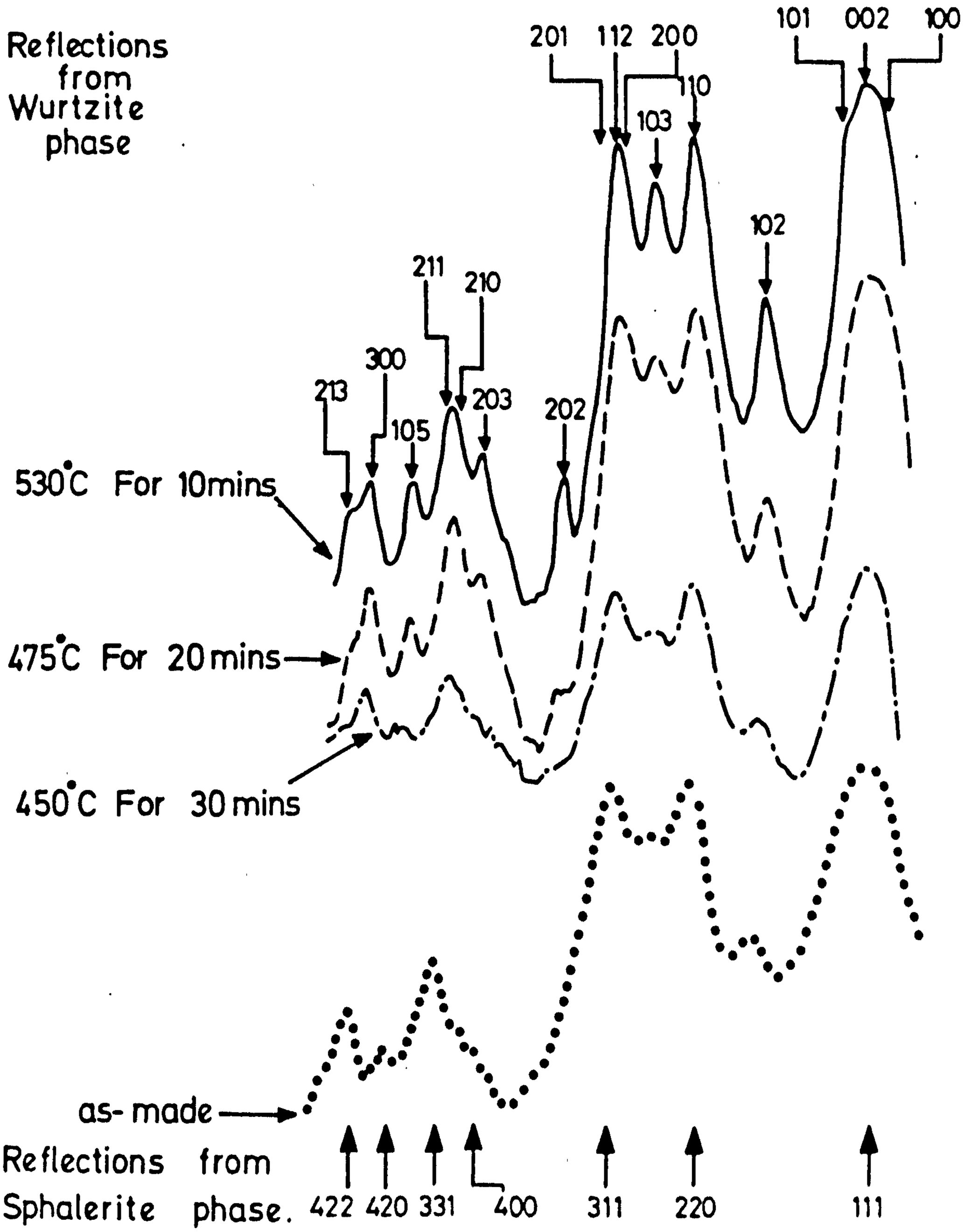


FIGURE 7.2: Densitometer traces taken from RHEED patterns from samples heat treated in argon for the periods and temperatures shown.

other wurtzite reflections they are clearly spaced from any of the reflections from the sphalerite phase. They can therefore be used as immediate indications of the presence of the wurtzite. The traces in Fig 7.2 show that the effect of increasing the annealing temperature was to increase the wurtzite content of the films. After 20 min heating at 475^{o}C, definite evidence of an increase in the intensities of the (102) and (103) reflections of the wurtzite structure relative to those of the sphalerite phase can be seen. The relative intensity of these two particular peaks reached their maximum value when the annealing temperature was increased to 530^{o}C in a reduced heating period of 10 mins. The RHEED pattern corresponding to this annealed sample is shown in Fig.7.3. Judging from the width of the various diffraction rings and the corresponding microdensitometer traces it can be inferred that no appreciable grain growth occurred during annealing up to this temperature. Heating above 550^{o}C led to so much material loss that reflections from the SnO_2 beneath the CdS became apparent in the diffraction pattern.

7.3.2 Electrical Properties

Coincident with the phase change produced by annealing at 530^{o}C there was a reduction in the resistivity of the film by more than two orders of magnitude. No reasonable measurements of resistivity could be obtained with films annealed at higher temperatures because of shunting paths. More detailed studies of the electrical properties were made by evaporating 1mm gold dots on to the CdS and then measuring the J-V and C-V characteristic of the resultant Schottky diodes. In general three types of J-V characteristics were obtained (Fig 7.4). These are designated as FC, GC and SC. FC corresponds to devices in which there was practically no current with forward bias up to 1 volt. The term S.C. corresponds to short circuited devices. Such behaviour is attributable to pin holes or cracks formed during the deposition or annealing. GC characteristics are those which give

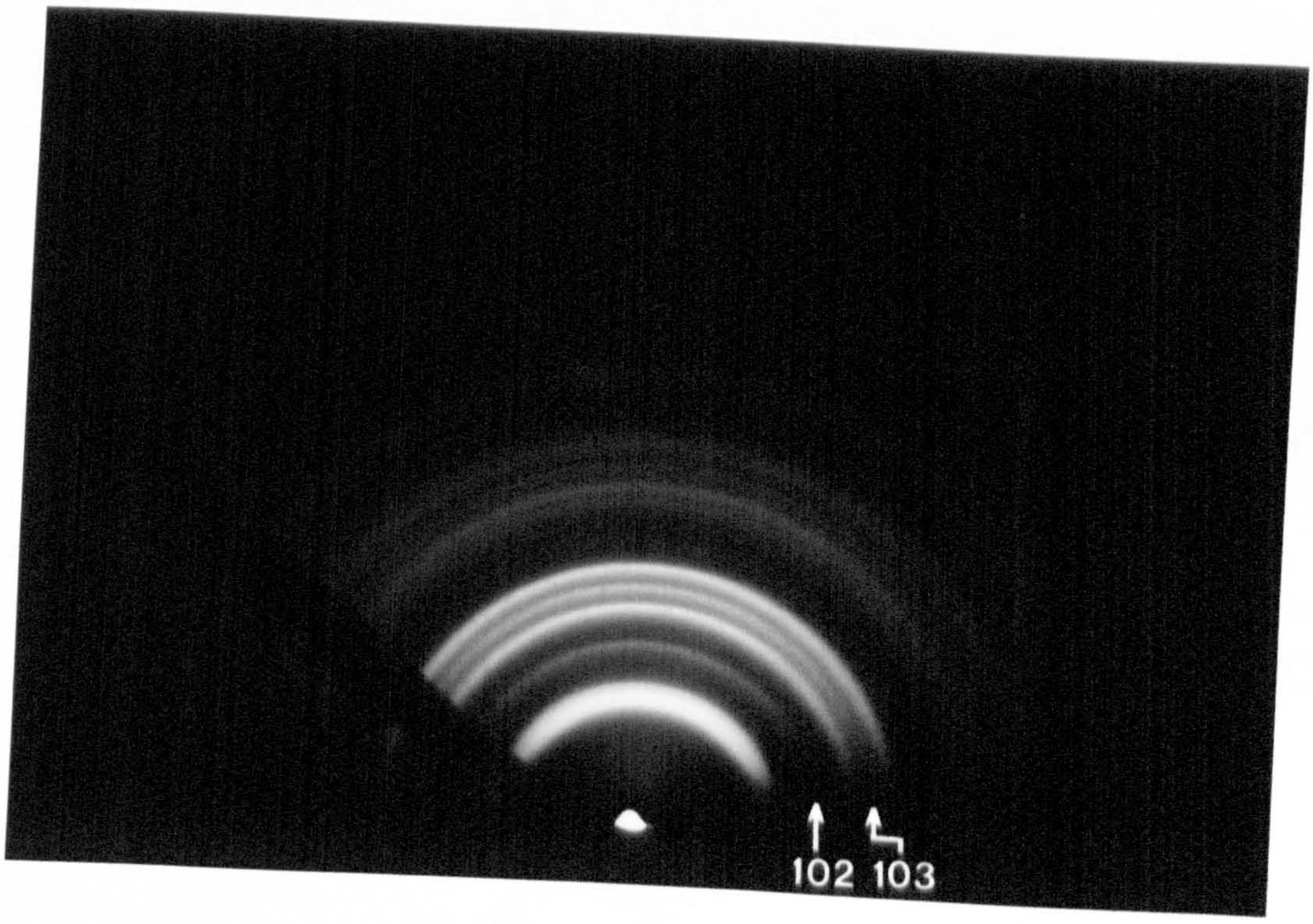


FIGURE 7.3: RHEED pattern from a film annealed at 530^{o}C for 10 min

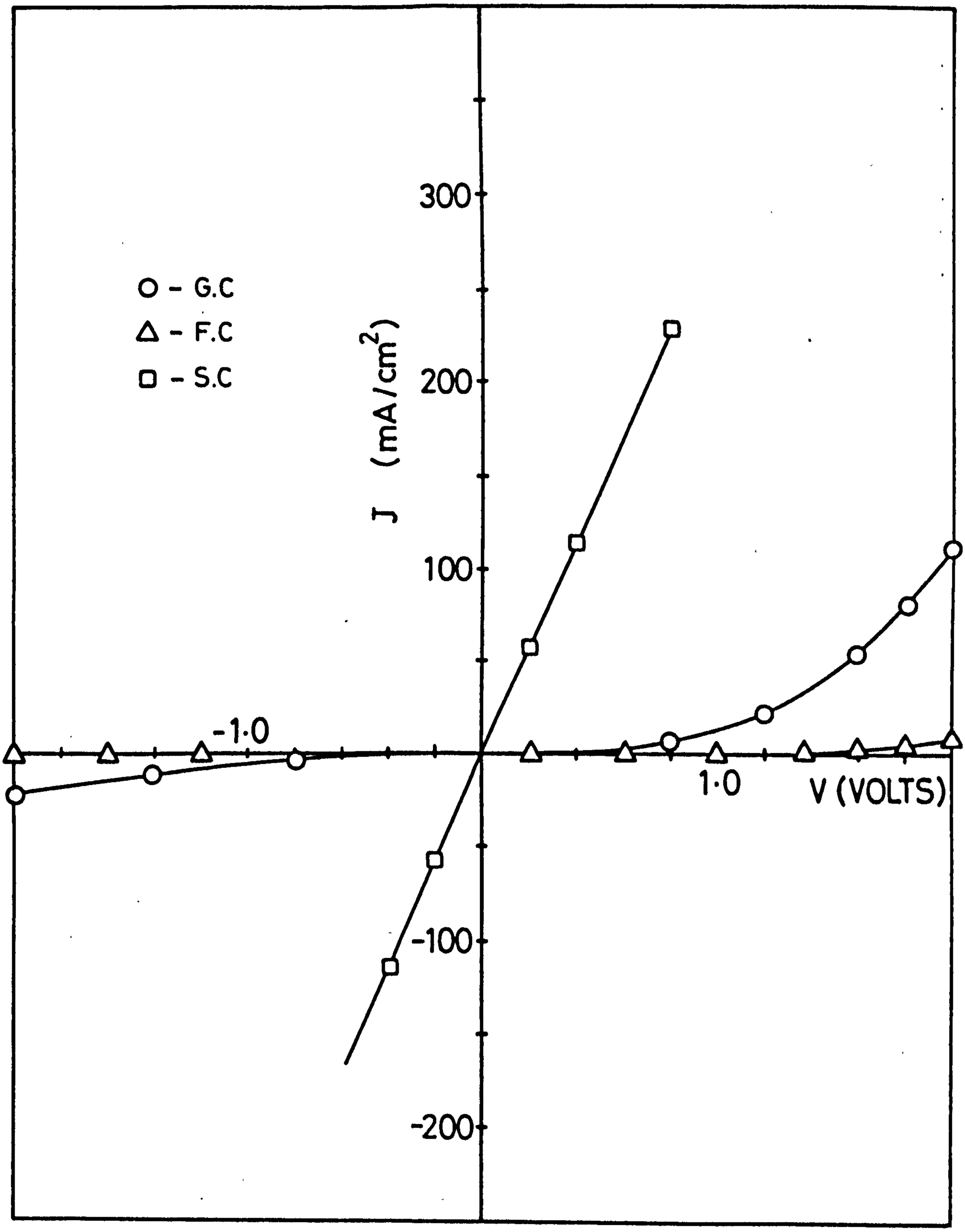


FIGURE 7.4: J-V characteristics for the Schottky devices on annealed binderless films

a normal Schottky rectifying characteristic, though the slope in the forward bias characteristic often indicated a high series resistance. GC characteristics were obtained with samples which were annealed at 475° C for 20 mins and at 530°C for 10 min, and even then the yield was very low. To increase the yield the diameter of gold dot contact was reduced to 0.5 mm.

The C^{-2} versus V plots gave a straight line in the region from -0.1 V to -1V. Fig 7.5 shows the curve for a device formed on a film which was annealed at 530°C for 10 mins. The slope of this line was used to determine the values of the uncompensated donor densities from the relation[12]

$$(N_D - N_A) = \frac{2}{q\ \varepsilon_o\ \varepsilon_S A^2} \frac{d(V)}{d\ (C^{-2})}$$

where A is the area of the gold contact.

A summary of the resistivities and the uncompensated donor densities obtained following different heat treatments in argon is provided in Table 7.2. The electron mobilities (μ) at room temperature were also calculated on the assumption that $\rho^{-1} \simeq (N_D - N_A) q \mu$

TABLE 7.2: Effect of Annealing in Argon

Annealing Temperature (° C)	Duration of Annealing (Min)	(N_D-N_A) cm^{-3}	Resistivity ohm-cm	(μ) $cm^2 V^{-1} s^{-1}$
350	90	-	$> 10^6$	
400	120	-	5×10^5	
450	30	-	10^5	
475	20	5.5×10^{14}	8×10^4	0.14
530	10	8.8×10^{15}	10^4	0.07

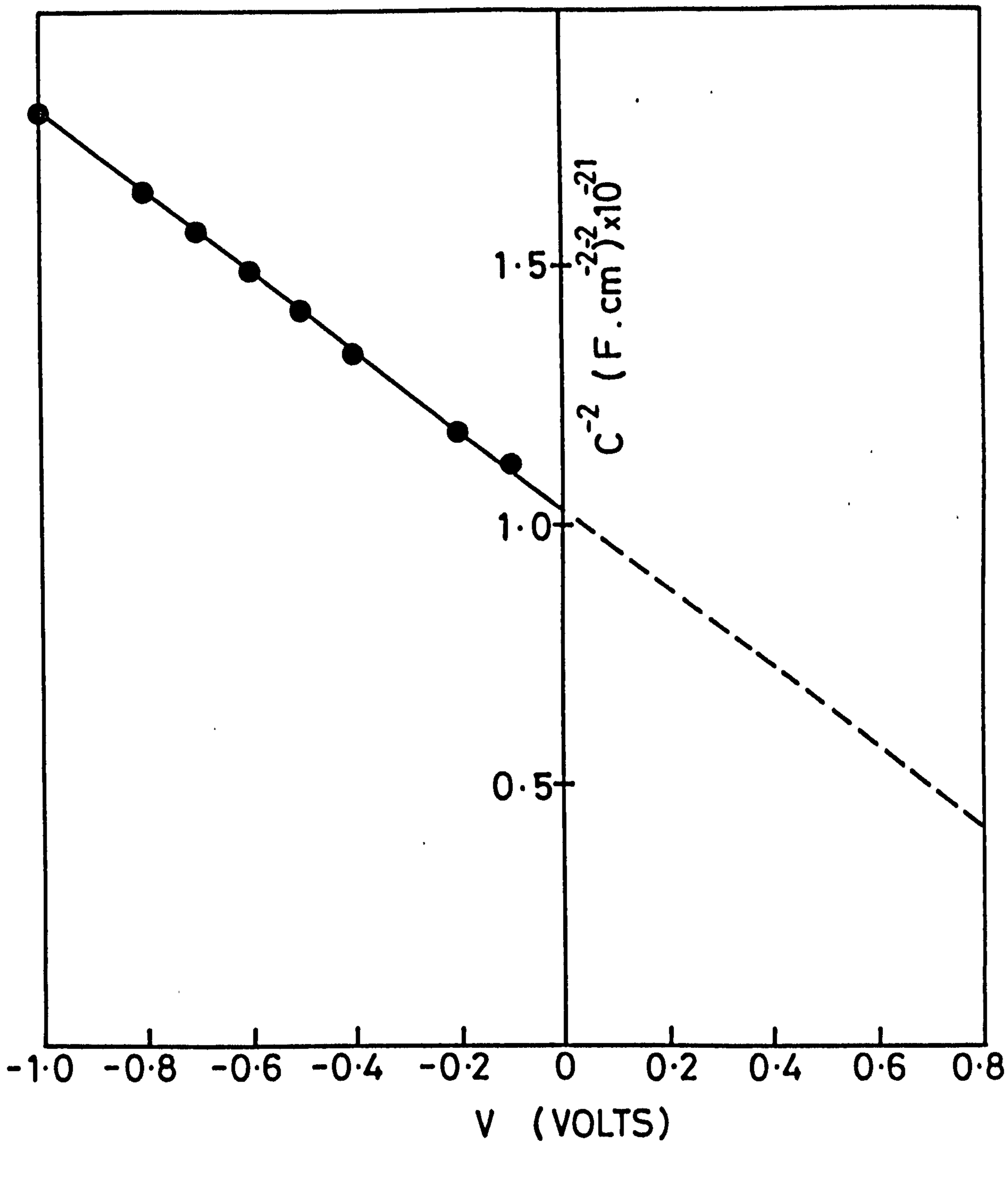


FIGURE 7.5: A typical C^{-2} -V plot for a Schottky device on a film annealed at 530°C for 10 min

The value of (N_D-N_A) could not be calculated for the samples annealed below 475° C because of their very high resistivities. Quenching trials led to the development of lots of cracks which led to short circuited devices.

Devices were also made on films which were annealed at 530°C for periods ranging from 10 min to 5 days, in vacuum, and in argon at 1/10 and 1/2 atmospheric pressure. These were compared with devices prepared from samples annealed in flowing argon. No remarkable difference was observed. As a result the annealing trials were carried out in a slow flow of argon (20 ml/min). The number of good Schottky devices which could be obtained from these binderless films was limited, and they were not suitable for heterojunction formation because short circuits developed. Moreover their resistivity was still quite high even after the optimum annealing. As a result annealing trials were carried out in the presence of halide fluxes since halogens are known to introduce donors in II-VI crystals[13].

7.4 HEATING WITH A HALIDE FLUX

The following different halides : CdF_2, NaCl, CdI_2, $ZnCl_2$ and $CdCl_2$ were considered. In separate trials a thin layer (about 100 Å) of each halide was vacuum deposited on to the CdS film which was then annealed in a stream of argon. The heating was performed in two stages. The first stage was carried out at low temperature (< 350 °C) depending upon the particular halide used. This was done from 90 min to 120 min. Subsequently the temperature was varied to an upper limit of 530°C for 10 minutes. The two stage process was necessary because direct heating at temperatures in excess of 400°C led to immediate re-evaporation of the halide.

Schottky devices were formed on the surfaces of all samples annealed in this way. The devices heated with $ZnCl_2$ and NaCl either gave FC or SC characteristics. A few devices formed on the sample treated with CdI_2 gave good J-V characteristics but the yield was poor and no proper C-V measurements could be made. Fortunately there was a considerable improvement in the yield from films treated with $CdCl_2$. Considering the limiting thick-

ness of the binderless films (1-2 μm) provided, it is difficult to be categorical about the relative effect of these different halides, however of those investigated $CdCl_2$ proved to be most effective.

7.4.1 Effect of Thickness of $CdCl_2$

To investigate in detail the effects of using $CdCl_2$, layers of this halide ranging from 50 to 400 Å thick were deposited on to separate sections of the same film. Each piece of the film therefore was given an identical heat treatment in argon at 350° C for 90 min and then at 530°C for 10 min. Schottky devices were made on each section and their J-V characterstics are shown in Figure 7.6. The device formed on the film treated with 50 Å of $CdCl_2$ shows a higher series resistance than that of the one formed on the film treated with 100Å of $CdCl_2$. On increasing the thickness of $CdCl_2$ the reverse bias leakage current progressively increased. On the device formed on the film treated with a layer 400 Å thick, the forward bias characteristic varied from point to point while the reverse bias characteristic gave rise to a breakdown at 0.1-0.2 volts. In addition to this, a white deposit was also observed on the films after heat treatment.

From these observations a layer of $CdCl_2$, 100 Å thick was chosen as the optimum to produce a substrate material with the most suitable properties. The good devices obtained with such $CdCl_2$ treated films had a much higher yield (> 75%) than those on films heat treated without $CdCl_2$ ($\tilde{<}$ 20%).

7.4.2 Effect of $CdCl_2$ Treatment on Structure

The RHEED investigations carried out on $CdCl_2$ treated samples are summarised in Fig 7.7, which shows the micro-densitometer traces of the patterns from the samples given the different treatments. The presence of $CdCl_2$ has a considerable effect on the temperature necessary to produce the transformation from the cubic to the hexagonal phase of CdS. By comparing these traces with those in Fig. 7.3, it can be seen that heating a film carrying a 100 Å layer of $CdCl_2$ at 450°C for 30 min led to a more complete

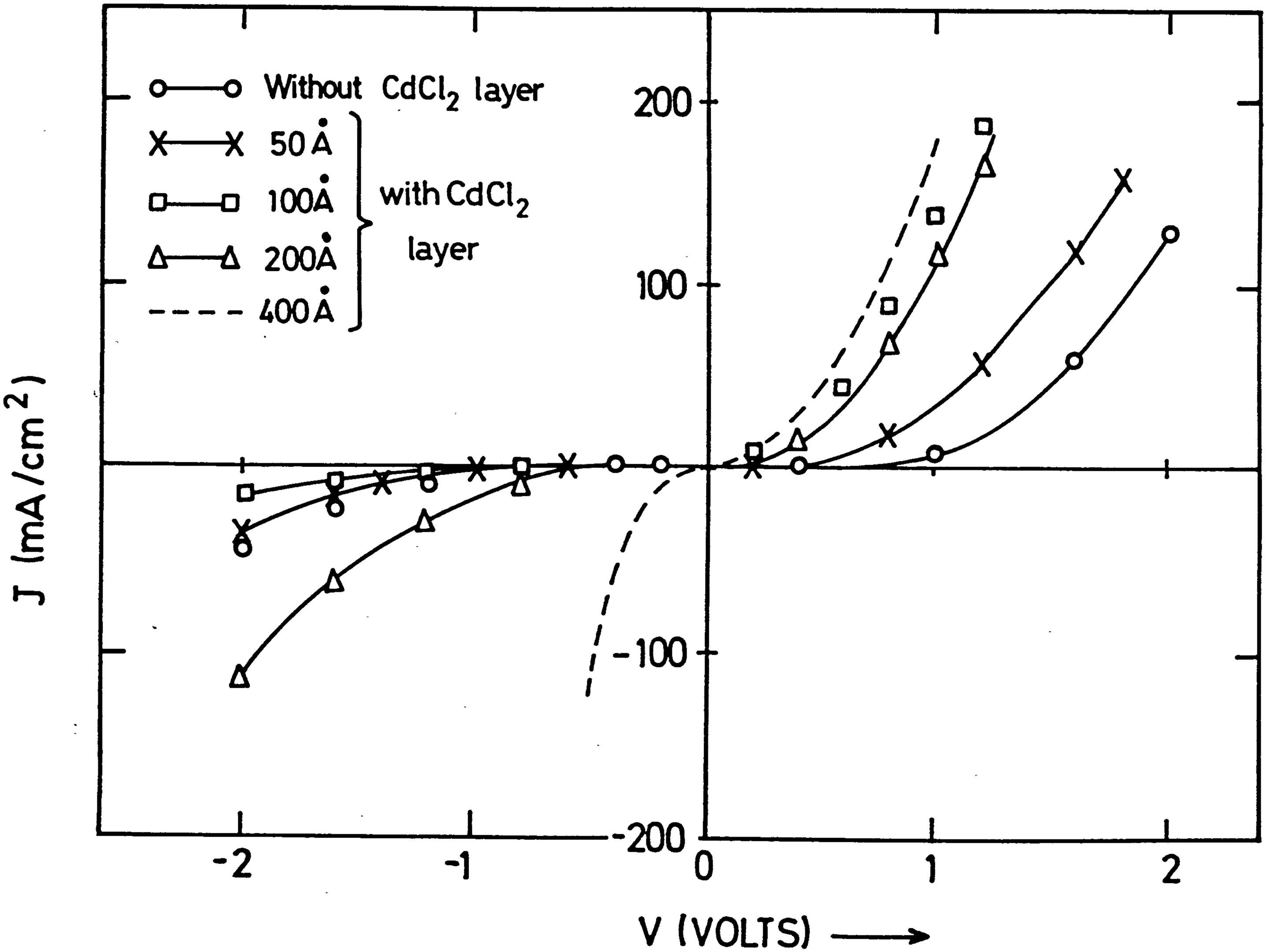


FIGURE 7.6: Schottky diode characteristics of films annealed at 530°C for 10 min after being coated with $CdCl_2$ layers of the thicknesses shown.

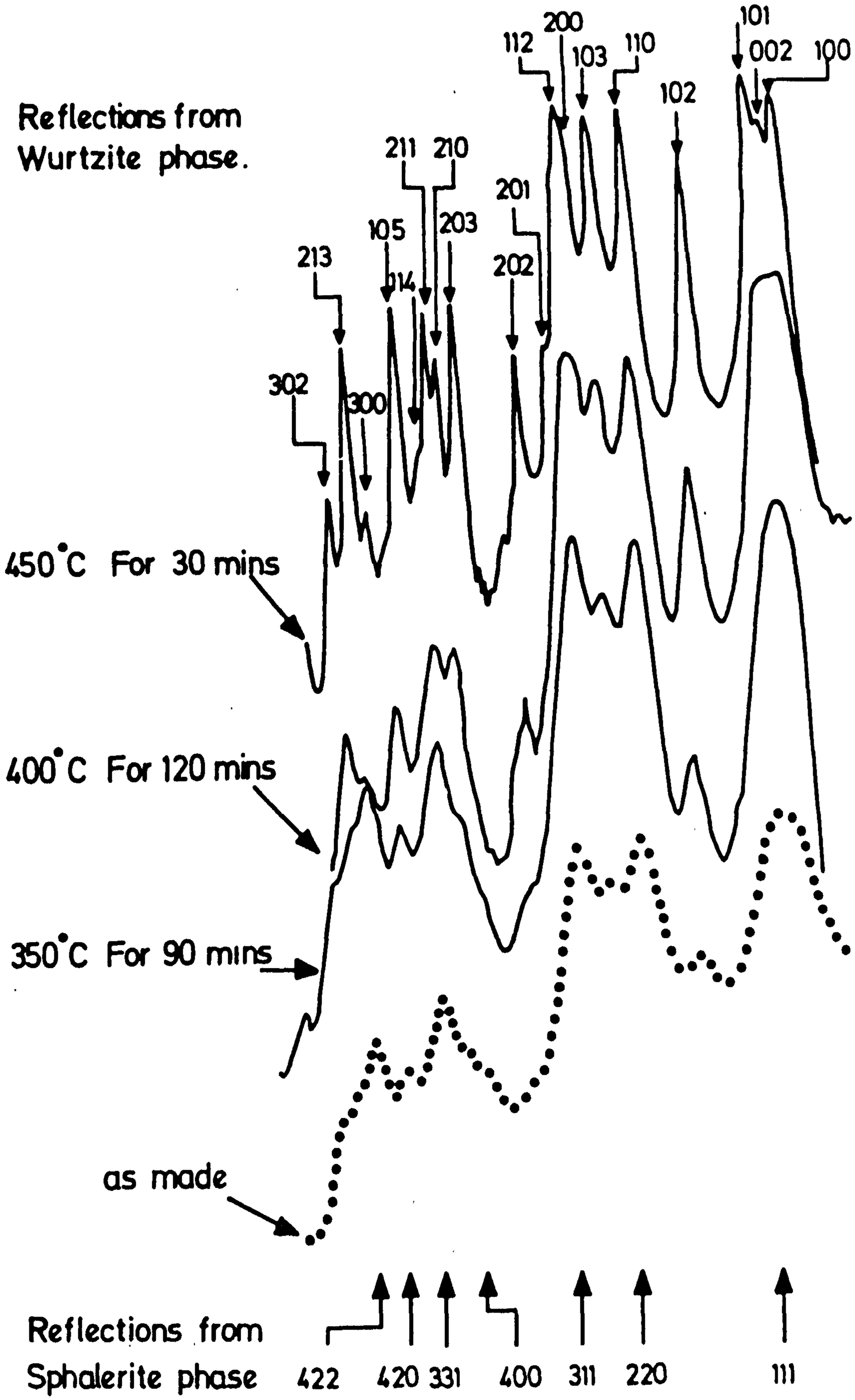


FIGURE 7.7: Densitometer traces taken from reflection electron diffraction patterns for samples with an overlayer of $CdCl_2$ after heat treatments as shown.

conversion to wurtzite, than heating an untreated film of CdS at 530°C for 10 min. The RHEED pattern of this $CdCl_2$ treated sample is shown in Fig 7.8 where the (102) and (103) diffraction rings corresponding to hexagonal phase can clearly be seen. To establish that the whole film had been converted to the hexagonal phase, some samples were etched with 1/10 HCl for a short time. The RHEED pattern of the etched samples confirmed that the films were hexagonal throughout. It is perhaps worth mentioning that when the phase changed the dark reddish yellow colour of the as-deposited film changed to buff yellow.

7.4.3 Effect of $CdCl_2$ Treatment on Electrical Properties

The variation of resistivity of a film with temperature and duration of annealing, is illustrated by the values in Table 7.3. The corresponding concentrations of uncompensated donor densities determined from C^{-2} - V plots are also indicated, together with the calculated values of electron mobility (μ) at room temperature. As the annealing temperature was raised above 400°C, it was essential to reduce the duration of the treatment in order to minimise material loss and reduce the incidence of pin holes.

TABLE 7.3: Effect of $CdCl_2$ Treatment on the Electrical Properties of E.D. CdS Films.

Annealing Temperature °C	Duration Time	N_D-N_A cm^{-3}	ρ ohm cm	μ $cm^2\ V^{-1}\ s^{-1}$
350	90	-	5×10^5	-
400	120	1.8×10^{14}	10^5	0.34
450	30	6.6×10^{15}	10^3	0.95
475	20	7.7×10^{15}	10^3	0.08
550	10	2.7×10^{16}	6×10^2	0.38

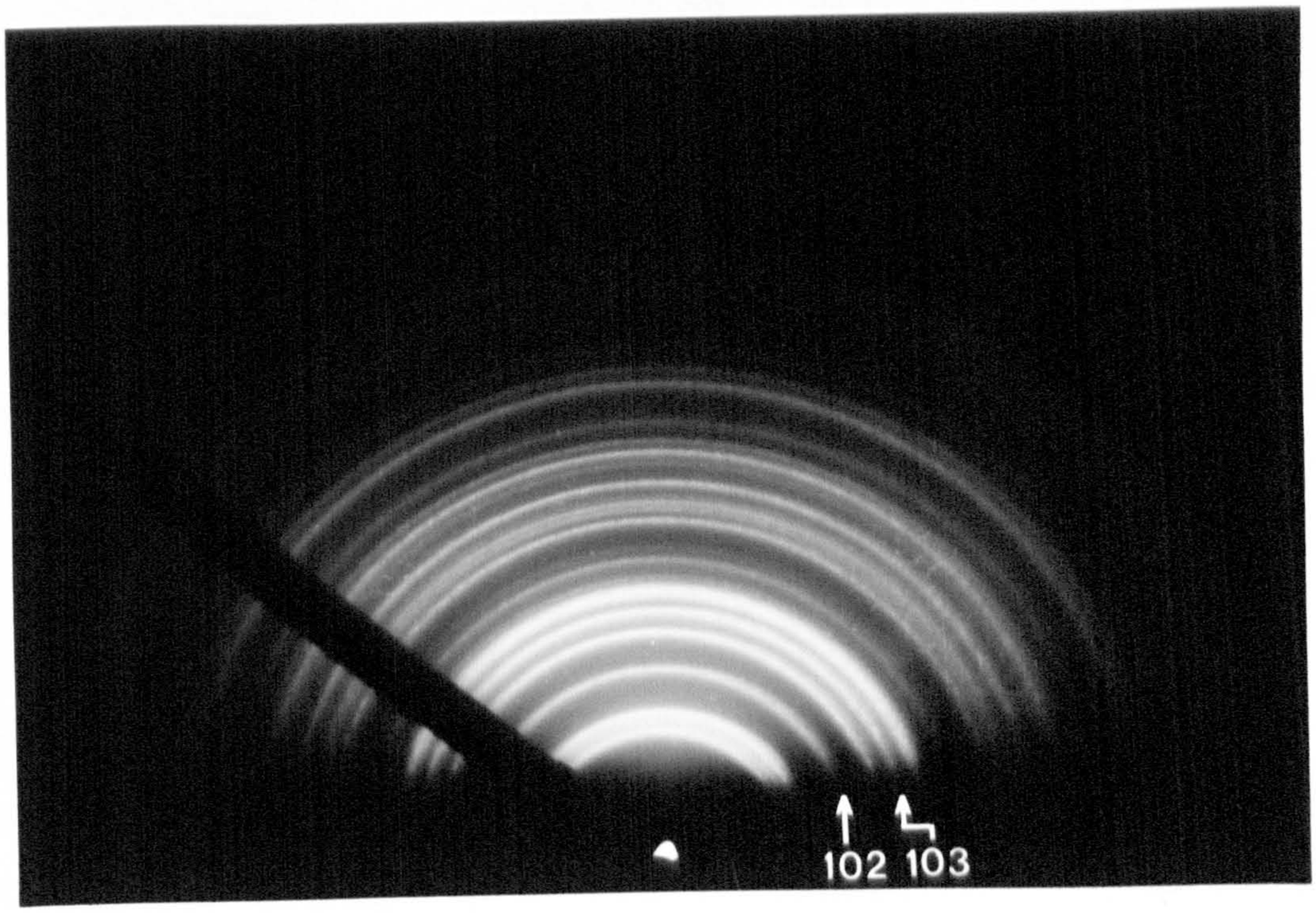


FIGURE 7.8: RHEED pattern from film annealed at 450°C for 30 min with an overlayer of $CdCl_2$

A comparison of these results with those recorded in Table 7.2, shows that the uncompensated donor concentration increased steadily as the annealing temperature was increased, whether or not an overlayer of $CdCl_2$ was present. However, a significantly higher donor concentration resulted when $CdCl_2$ was used, together with a correspondingly lower resistivity. The values of electron mobility exhibit considerable scatter with no discernible trend. Most values lay in the range 0.1-1.0 $cm^2\ V^{-1}\ s^{-1}$ which is substantially lower than that for a bulk single crystal of 300 $cm^2\ V^{-1}\ s^{-1}$. The C^{-2} - V plots were straight lines in the region of - 0.1 - 1 volt. A typical graph (Fig 7.9) is shown for the device formed on a film annealed at 450°C for 30 min. The intercept on the x-axis of the extrapolated line of this plot which gives V_d, sometimes (Fig 7.5) showed values larger than 1V which suggests that some interfacial layer[13,14] might have developed during heat treatment.

7.5 PHOTOCAPACITANCE MEASUREMENTS

Steady state photocapacitance spectra of the Schottky diodes were measured at 85K as the incident monochromatic light was scanned very slowly from long to short wavelengths. The curves shown in Fig 7.10 are for diodes on the two halves of a layer (i.e. with and without $CdCl_2$) after annealing at 530°C for 10 min . A sudden increase in capacitance (Δ C positive) indicates the onset of a process in which the incident photons eject electrons from filled levels to the conduction band. Similarly a sudden decrease (Δ C negative) indicates the onset of transitions from the valence band to empty levels. The curves in Fig 7.10 both exhibit positive going thresholds at about 1.55 and 2.3 eV. In addition the diode on the film treated with $CdCl_2$ shows a small negative threshold at about 1.0 eV and a stronger one at 2.2 eV. There is also a more pronounced peak in the vicinity of the CdS band gap at 2.5 eV.

For comparison purposes, photocapacitance curves were also obtained for Schottky diodes prepared on single crystal CdS (Fig 7.11). In this figure,

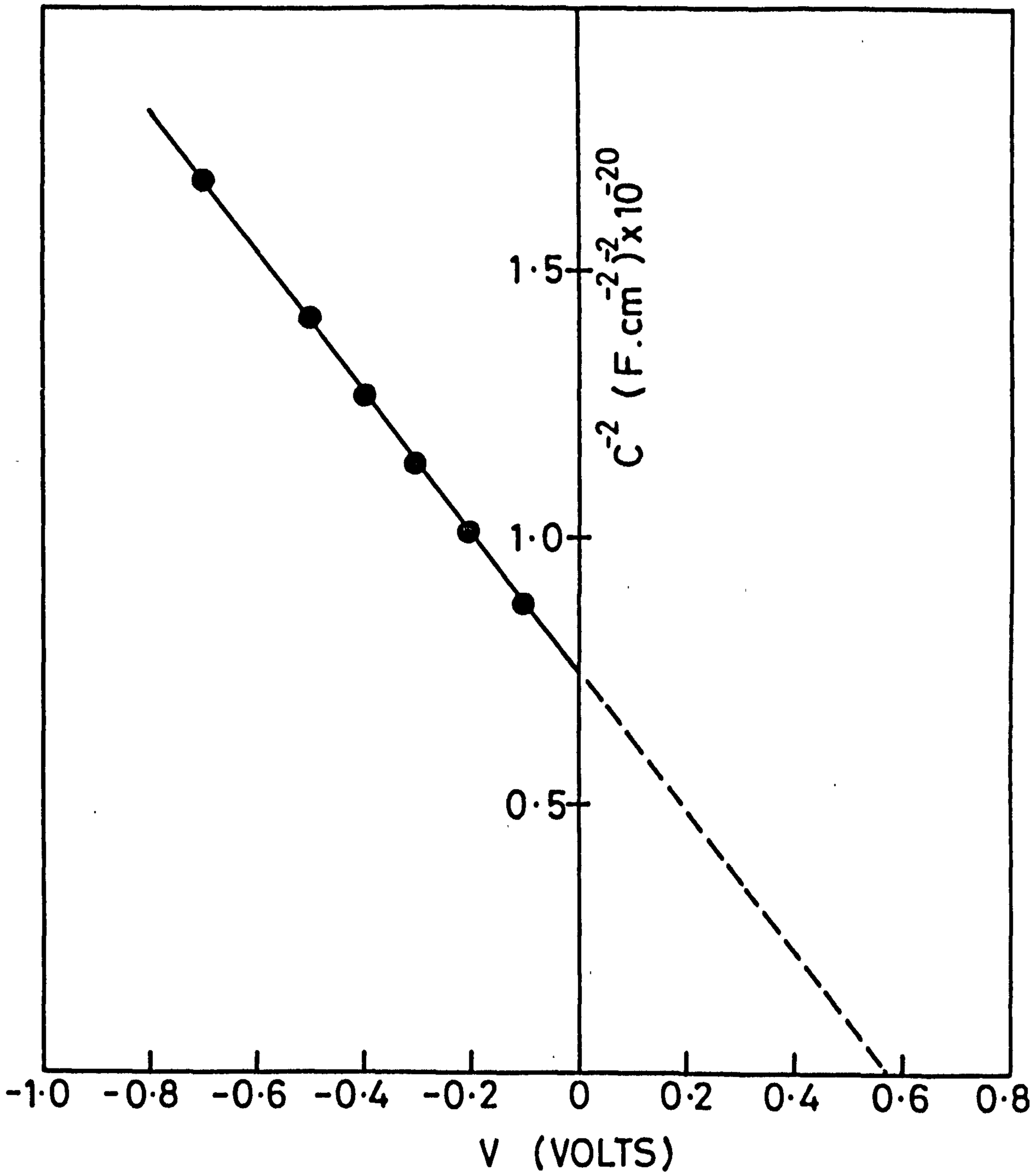


FIGURE 7.9: A typical C^{-2} - V plot for a Schottky device on a film annealed at 450°C for 30 min with an overlayer of $CdCl_2$

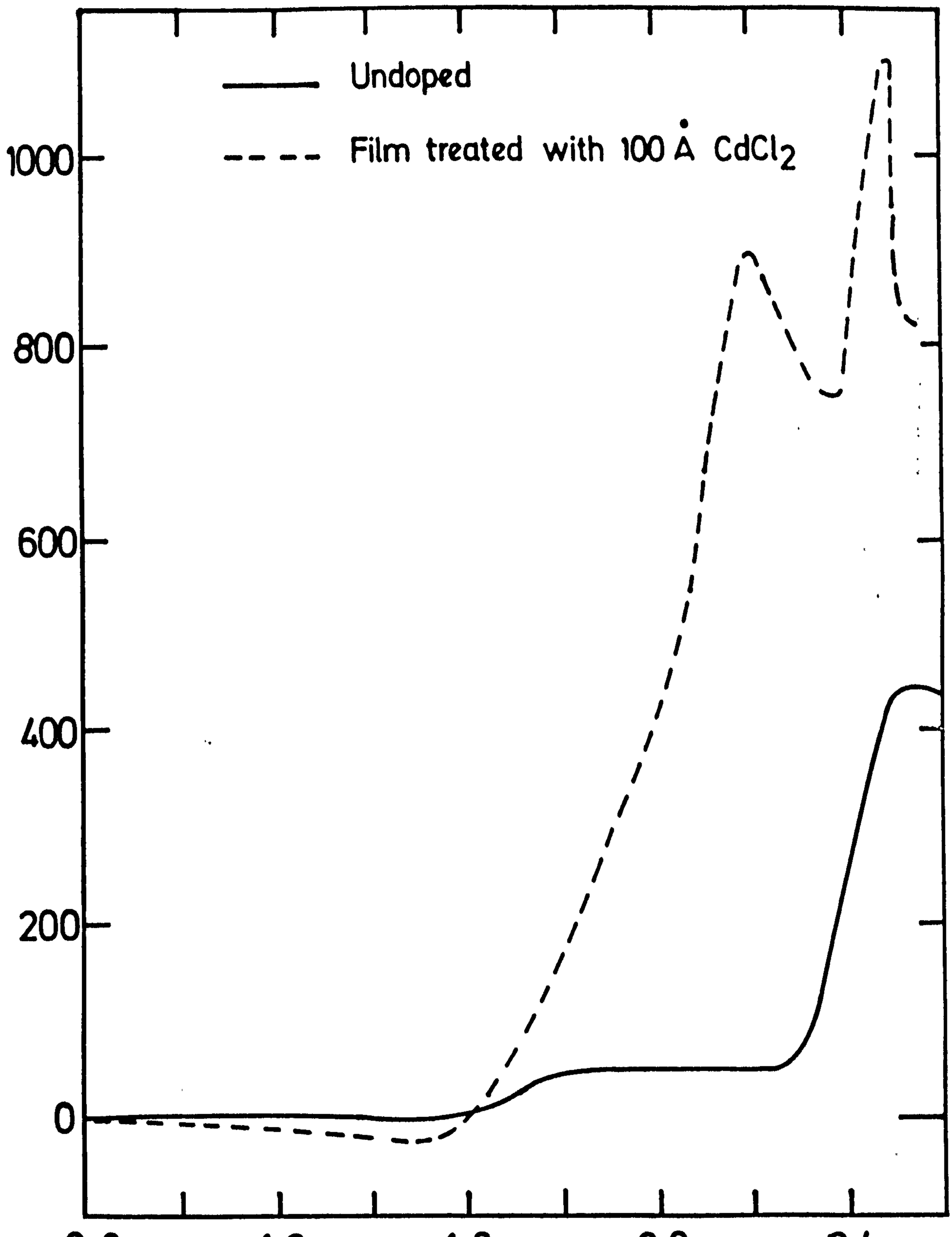


FIGURE 7.10: Photocapacitance curves for Schottky diodes on CdS films with and without $CdCl_2$ after an optimum annealing treatment.

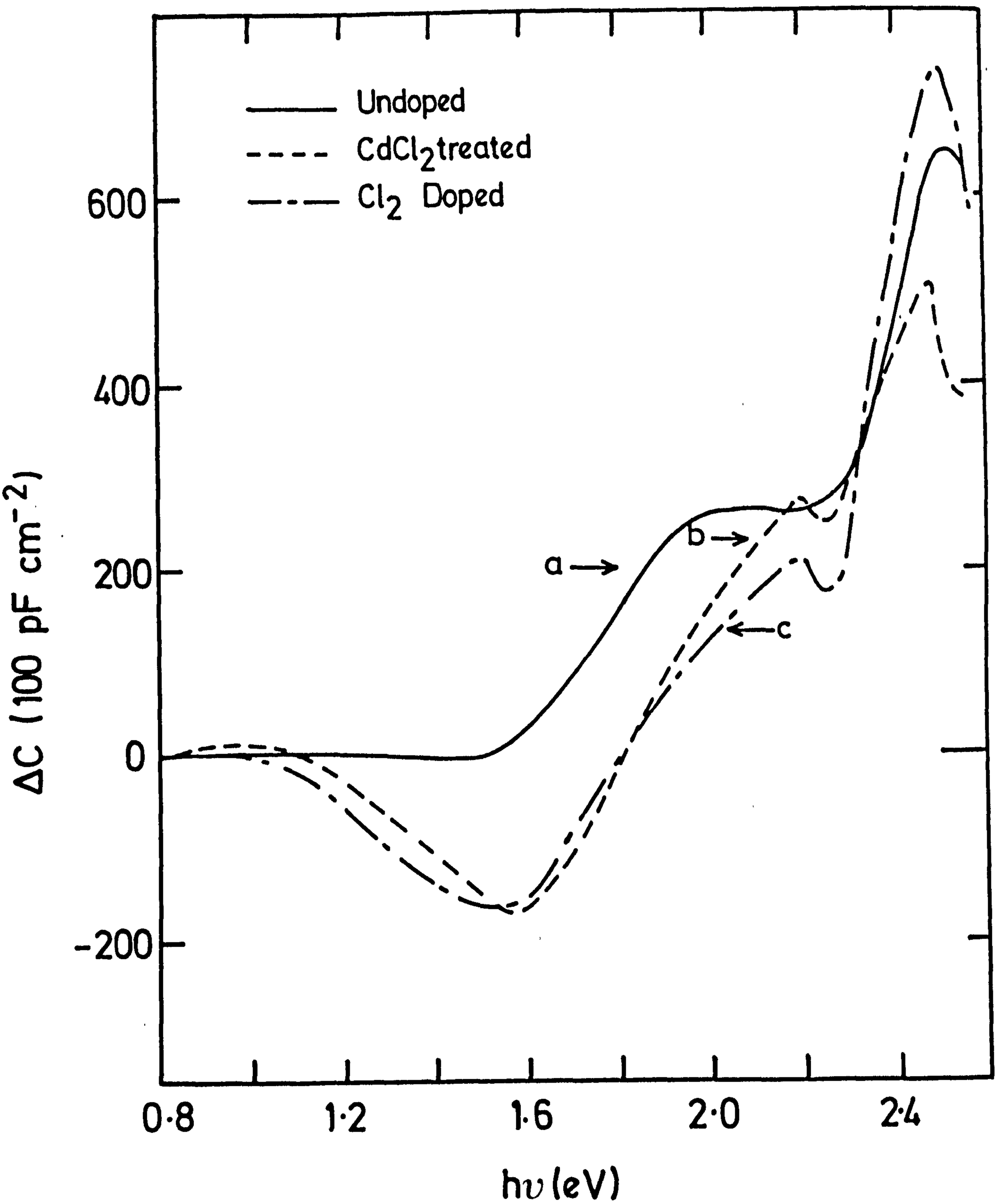


FIGURE 7.11: Photocapacitance curves for Schottky diodes on CdS single crystals (a) undoped (b) with an overlayer of $CdCl_2$ and an optimum anneal, and (c) with grown-in chlorine

curve a is for a diode on low resistivity, undoped CdS ; curve b is for a diode on the same material after a 100 Å film of $CdCl_2$ had been deposited and the optimum annealing treatment carried out ; and curve c is for a diode prepared on a crystal of CdS containing grown in chlorine. The curves are clearly similar in most respects to those of Fig 7.10, except that the negative going thresholds near 1.0 eV are much more pronounced with the single crystal devices. The negative thresholds at 2.2 eV are again prominent in the chlorine doped material.

7.5.1 Discussion on the Photocapacitance Studies

In the photocapacitance curves (Fig 7.10) for the films annealed with and without over layers of $CdCl_2$, the magnitudes of the two responses are about the same for the thresholds at 2.3 eV, but the response beginning at 1.55 eV is much larger in the device on the layer treated with $CdCl_2$. It is suggested that this latter threshold is associated with the excitation of electrons to the conduction band from levels 0.93 eV above the valence band, and that these levels are due to cadmium vacancies, which would be more numerous in chlorine doped CdS for reasons of charge compensation. The threshold at 2.3 eV corresponds to optical excitation to the conduction band of electrons from a level 0.18 eV above the valence band. Acceptor levels attributed to trace impurities of lithium and sodium, which are responsible for the well known donor-acceptor pair band edge emission, have very similar energies[14], It is tempting therefore to assign the positive change in ΔC which begins at 2.3 eV, and which is equally strong in both types of films, and in the single crystals, to common alkali-metal impurities.

In the devices made on films and crystals with chlorine there were three possible thresholds for negative-going photocapacitance effects. Of these, that at 1.0 eV was much the more pronounced in the single crystal devices, and importantly non-existent in the devices on untreated films and crystals. It is concluded therefore that the effect is associated with chlorine doping, and that the effect is due to the excitation of electrons

from the valence bands to levels 1.0 eV above the valence band and which are due to the complex of a cadmium vacancy and chlorine substitutional impurity on neighbouring lattice sites. Such a complex is of course the acceptor component of the donor-acceptor pair responsible for the self activated luminescence emission in chlorine doped CdS.

The negative-going threshold at 2.2 eV, observed only in chlorine doped devices, is attributed to a deep donor 0.28 eV below the conduction band. The capacitance is reduced when the donor level is filled with electrons excited from the valence band. It has often been suggested that two donor levels are associated with substitutional chlorine[15]. The first is the well known shallow level 0.028 eV below the conduction band. The second is less well attested and has variously been reported as some 0.26 eV below the conduction band. It is suggested therefore that the deep donors observed in this investigation is indeed the second chlorine level.

Whether or not the sharp decrease in photocapacitance at about 2.48 eV is associated with the filling of the shallow chlorine donor levels with electrons from the valence band is less clear, since thermal excitation of electrons from such levels must be quite rapid. Nonetheless some freeze-out of electrons into such shallow donors is observed in Hall measurements and Marfaing et al[16] and Qidwai and Woods[17] claim to have observed similar photocapacitance effects involving shallow donors in CdTe and ZnSe.

7.6 HETEROJUNCTION DEVICES ON THIN FILMS

After characterising the electrical and structural properties of these thin films, heterojunctions were prepared on them by the dry barrier process. Reasonable devices could only be obtained by depositing a very thin layer of CuCl (600 Å) and heating in argon at 200°C for 2 min. It was also necessary to limit the area of the junction by using a small aperture (1.4 mm dia) mask. The J-V characteristics of such a device measured both in the dark and under AM 1 illumination are shown in Fig 7.12. Values of OCV = 0.4V and

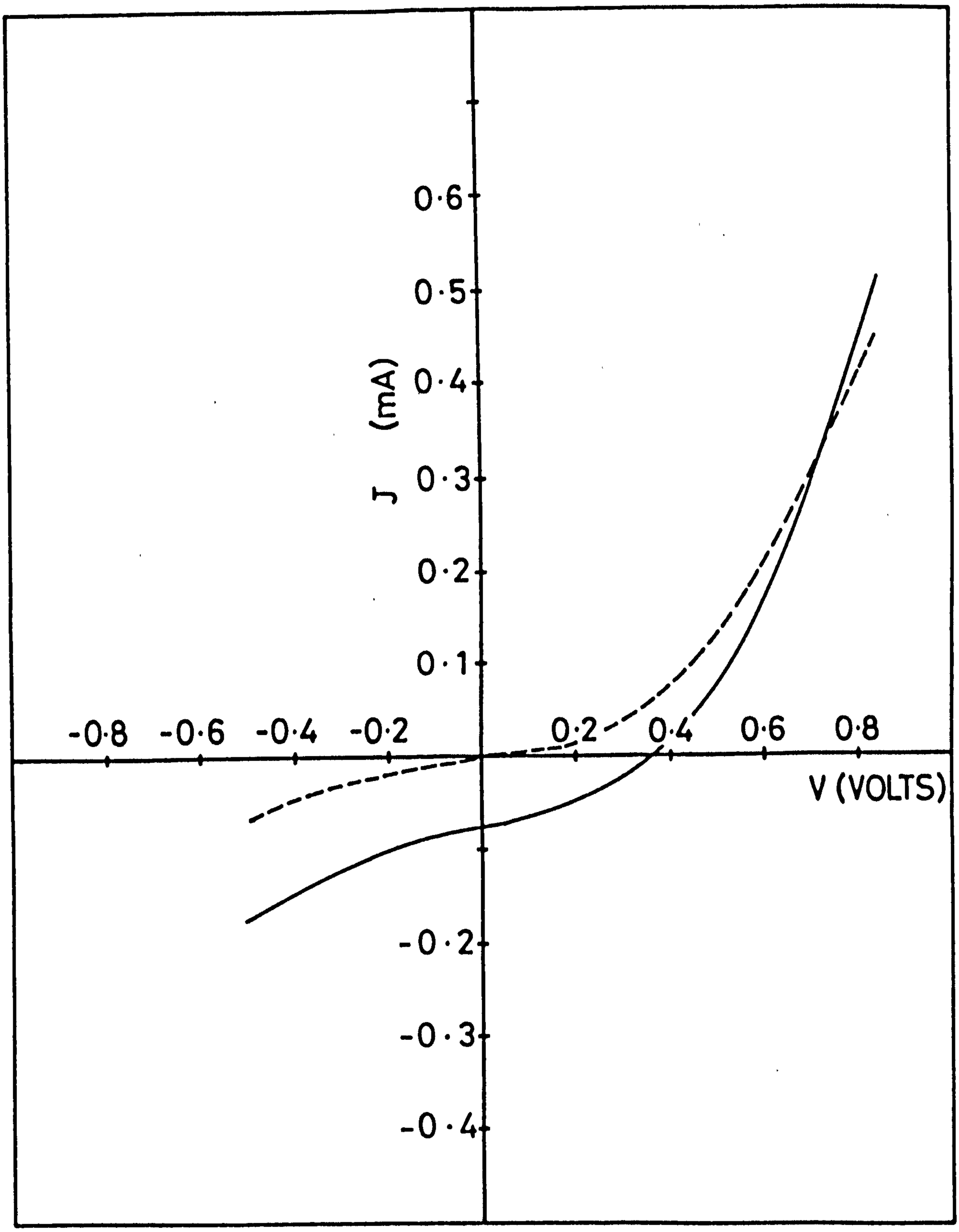


FIGURE 7.12: J-V characteristics of a heterojunction (d = 1.4 mm) formed on a thin film

[___ dark characteristics

.... light characteristics]

SCC = 0.095 mA (6.2 mA/cm^2) were obtained, which degraded to OCV = 0.35V and SCC = 0.065 mA, within 24 hours. The rate of degradation subsequently decreased and after two weeks the following values were obtained, OCV = 0.33V and SCC = 0.056 mA. Although the J-V characteristics were not very good, this was the best working device obtained on the very thin binderless layers[18]. The main reason for the low values of the SCC is attributable to the high resistivity of the CdS, and inadequate thickness of the Cu_xS layers.

The spectral response of the OCV of a typical device is shown in Fig 7.13. The major response at 0.68 μm can be attributed to the copper levels in the CdS[19]. This is consistent with the fact that the layer of copper sulphide on the cell was expected to be very thin and the main response was comparable to the spectral response obtained from the devices formed on single crystal substrate with a thin layer of CuCl[20]. Attempts to prepare devices on these thin films with thicker layers of CuCl led to short circuited junctions. Moreover the area of the devices was also limited. At this stage it was decided that it was essential to increase the thickness of the base CdS if efficient heterojunctions were to be prepared.

7.7 THICKER FILMS

The earlier attempts to increase the thickness of the binderless films led to the formation of numerous cracks (Fig 7.14). A considerable advance was made when the limit to the thickness of the deposited layers was removed by incorporating a small quantity of polyvinyl pyrolodine (PVP) in the plating bath. It was then possible to produce crackfree films up to 10 μm thick[21]. Two different sources of CdS were used for depositing these films. These were (a) flocculated CdS (redispersed CdS) and (b) CdS obtained from Johnson Matthey which was hexagonal. In a few samples the film was found to be non-uniform being thicker at the sides of the glass substrate than at the centre. This was attributed to the electric field varying across the substrate. Work was carried out on uniform samples only. The PVP

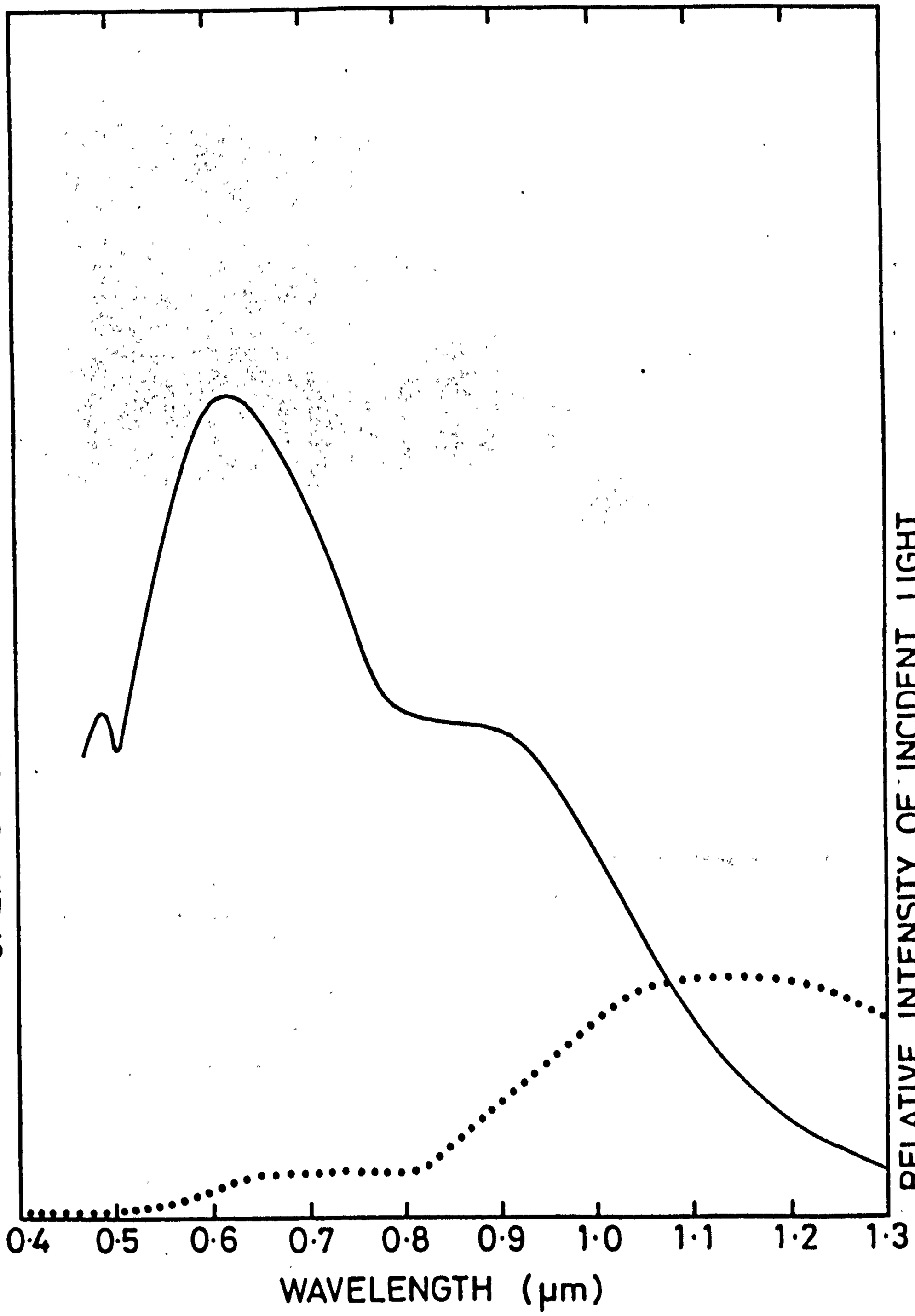


FIGURE 7.13: Spectral response of the OCV of a heterojunction formed on thin film

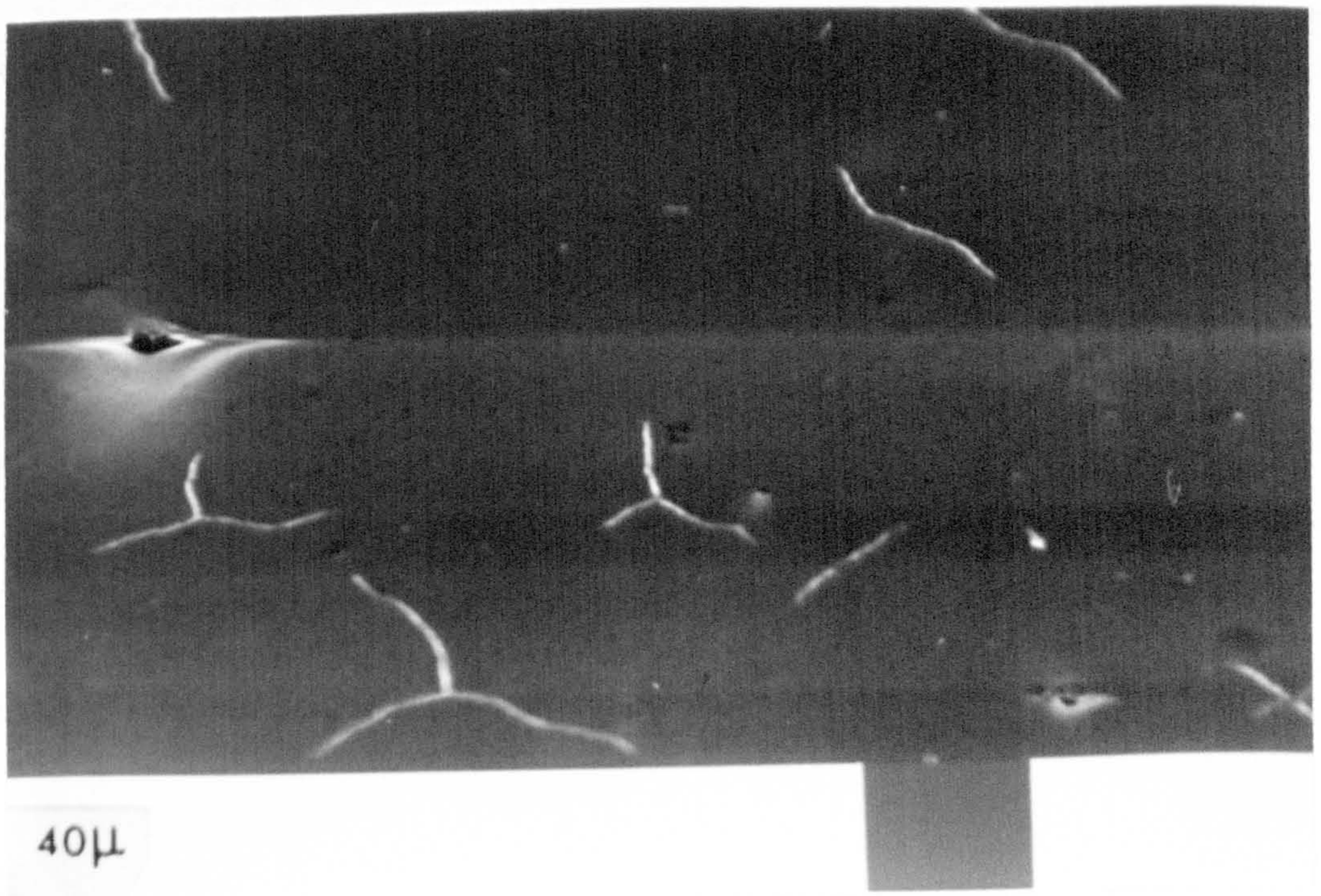


FIGURE 7.14: S.E. micrograph of thicker binderless films showing numerous cracks.

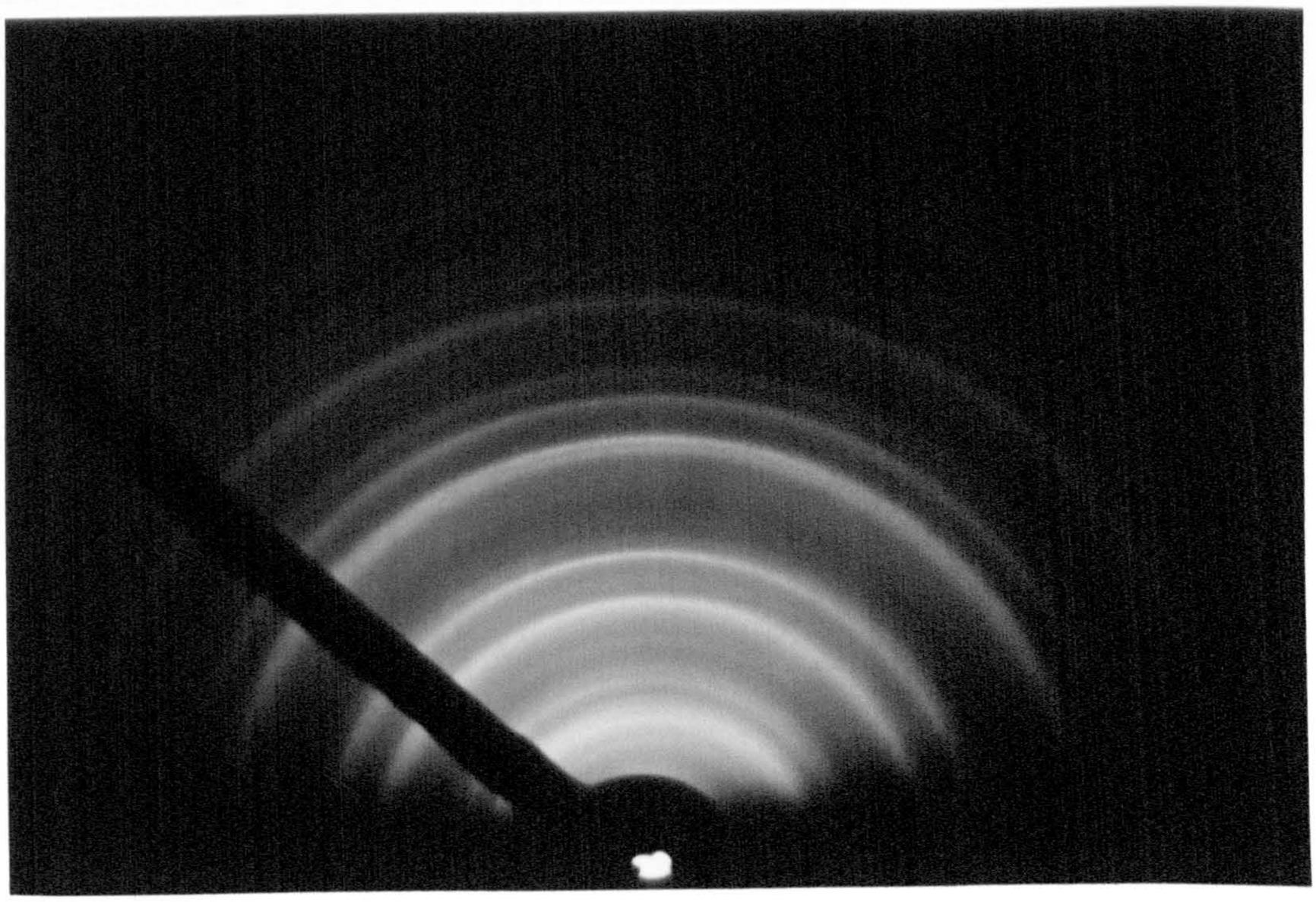


FIGURE 7.15: RHEED pattern for a film annealed in air at 400^{o}_{C} for 30 min

probably had deleterious effects on the properties of the films because heat treatment in argon turned them black. The films were therefore first heated in air to oxidise the polymer before subjecting them to the main heat treatment in argon at higher temperatures. In order to determine the treatment necessary to oxidise the PVP, while not adversely affecting the CdS, annealing trials were carried out in air over a range of temperatures and times. It was found that annealing the film at 350^{o}C for 90 min removed the PVP successfully. Temperatures higher than 350^{o}C led to the formation of CdO which was detected by RHEED studies (Fig 7.15). The d spacings calculated from this RHEED pattern are compared with those obtained from the ASTM index of CdO in Table 7.4 and are in good agreement. No such lines were found in the RHEED pattern of the film annealed at 350^{o}C, though no chemical test was performed to establish that the PVP was completely removed at this temperature. Certainly no blackening of the surface took place when the film was subsequently heated in argon. This was taken as an indication of the removal of PVP and as a result a treatment at 350^{o} C for 90 min in air was adopted for this purpose.

The resistivity of these polymer modified films was found to be noticeably higher (> 10^{7} Ω cm) than that of the films without PVP. In order to reduce the resistivity, they were given a $CdCl_2$ treatment similar to that described in section 7.4.6. After annealing, the resistivity of the films prepared from flocculated CdS was found to be one order of magnitude higher than that of those containing no PVP. The temperature limit was increased from 530^{o}C to 560^{o}C, and further reduction in the resistivity to a value of 10^{3} Ωcm was obtained. The films prepared from CdS purchased from Johnson Matthey were found to be highly resistive ($\rho = 10^{5}$ Ω cm). With these the resistivity could only be brought down further by depositing a thin layer of $InCl_3$ and subsequently heating in argon. This reduced the resistivity of these films to 10^{4} Ω-cm.

Ring	Measured Radius	Estimated Intensity	Measured d-spacing Å	ASTM DATA CdO d-spacing Å	ASTM DATA CdO Relative Intensity %
R_1	1.65	m	3.34		
R_2	1.9	s	2.90		
R_3	2.05	m	2.69	2.712	100
R_4	2.15	m	2.565		
R_5	2.35	s	2.35	2.349	88
R_6	2.5	w	2.21		
R_7	2.85	m	1.935		
R_8	3.15	m	1.75		
R_9	3.3	vs	1.67	1.661	43
R_{10}	3.55	m	1.55		
R_{11}	3.9	vs	1.41	1.416	28
R_{12}	4.1	m	1.345	1.355	13
R_{13}	5.1	s	1.08	1.0772	9
R_{14}	5.25	vs	1.05	1.0499	13
R_{15}	5.75	s	0.959	0.9584	11
R_{16}	6.1	s	0.904	0.9036	9

TABLE 7.4: Indexing of Pattern from Electrophoretic CdS after Thermal Annealing in Air

Heterojunctions were made on these films and their areas were increased by depositing CuCl through a mask with an aperture of 4 mm diameter. The thickness of the CuCl deposited was 1000 Å and a heat treatment at 200°C for 2 min was given to provide the solid state reaction. The J-V characteristics shown in Fig 7.16 are from devices formed on films prepared from the two different sources of CdS. In both the cases the OCV of the as-made device was ∿ 0.4 volt. The SCC was much smaller in the device formed on Johnson Matthey material which is attributed to the high series resistance indicated by the slope in the forward bias characteristics.

The spectral responses of the OCV of these devices are shown in Fig 7.17. The peak at 0.96 μm indicates the presence of chalcocite in both devices, though the device formed on Johnson Matthey CdS gave a much longer signal at 0.96 μm. This might be due to the fact that the Johnson Matthey CdS had the hexagonal structure in the as-grown state.

7.7.1 Treatments with Indium

Indium was incorporated in some films in an attempt to produce more conducting CdS[22,23]. Indium doped CdS powders with an indium content ranging from 0.001 to 0.5 mol % were produced (see Chapter 8, section 8.2). A powder of particle size $\tilde{\sim}$ 1 μm was obtained by swing milling the doped phosphor for 15 min. When this material was used in the process of electrophoretic deposition with PVP in the sol, much thicker films ($\tilde{\sim}$ 10 μm) containing up to 0.13 mol % indium could be deposited[24]. An S.E. micrograph of a fractured edge of such a film is shown in Fig 7.18. The RHEED pattern of this film is shown in Fig 7.19 which clearly indicates that the films in their as-deposited state were predominantly cubic. After the PVP was removed at 350°C for 90 min the films were mechanically soft. Their resistivity was very high ($> 10^7$ Ω cm) and treatment with $CdCl_2$ was initiated. The effects of the indium concentration and of the annealing temperature on the resistivity are shown in Table 7.5 (a) and 7.5 (b).

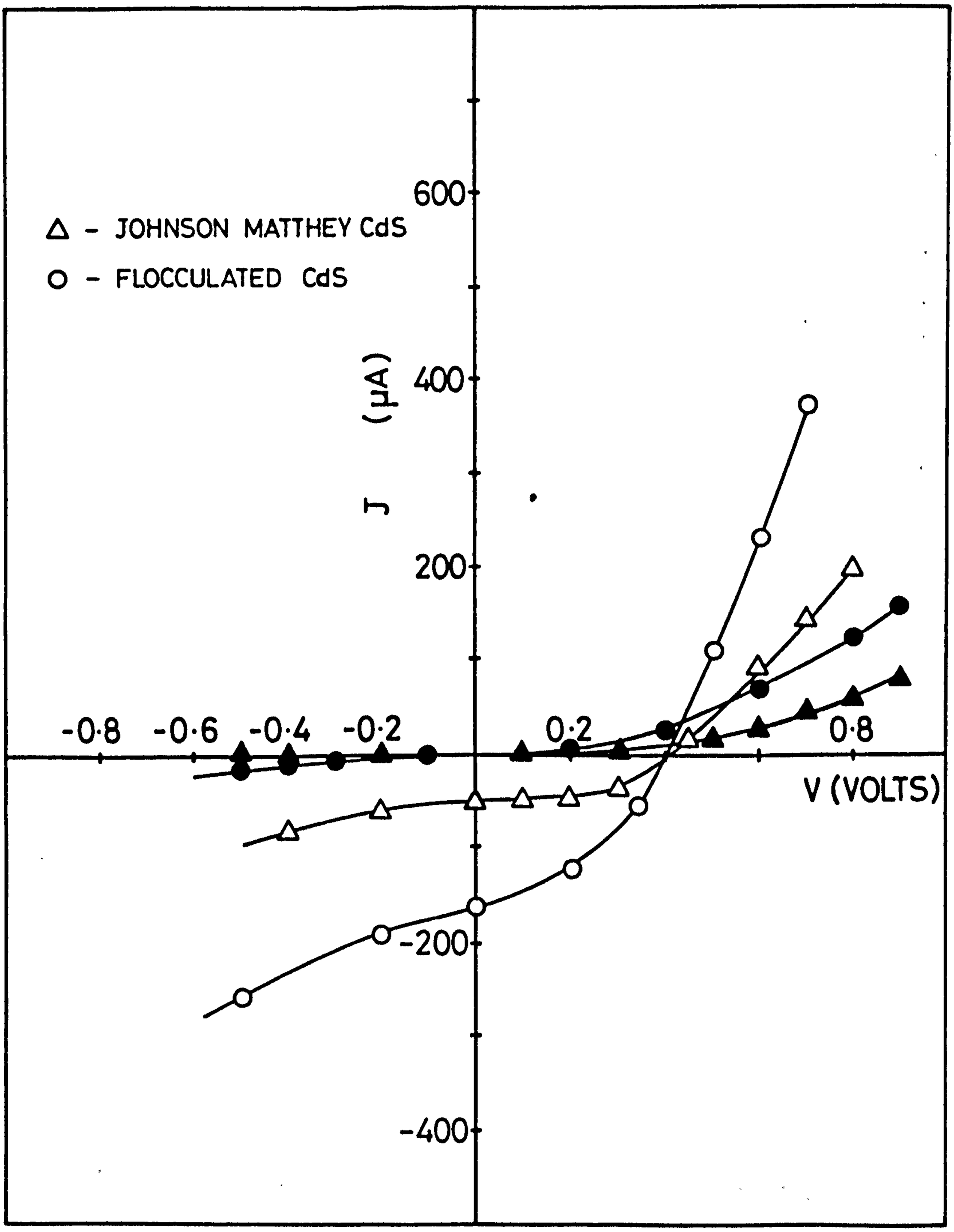


FIGURE 7.16: J-V characteristics of heterojunctions (d = 4mm) formed on electrophoretically deposited films prepared from different sources of CdS (open symbols - under AM 1 illumination filled symbols- in dark)

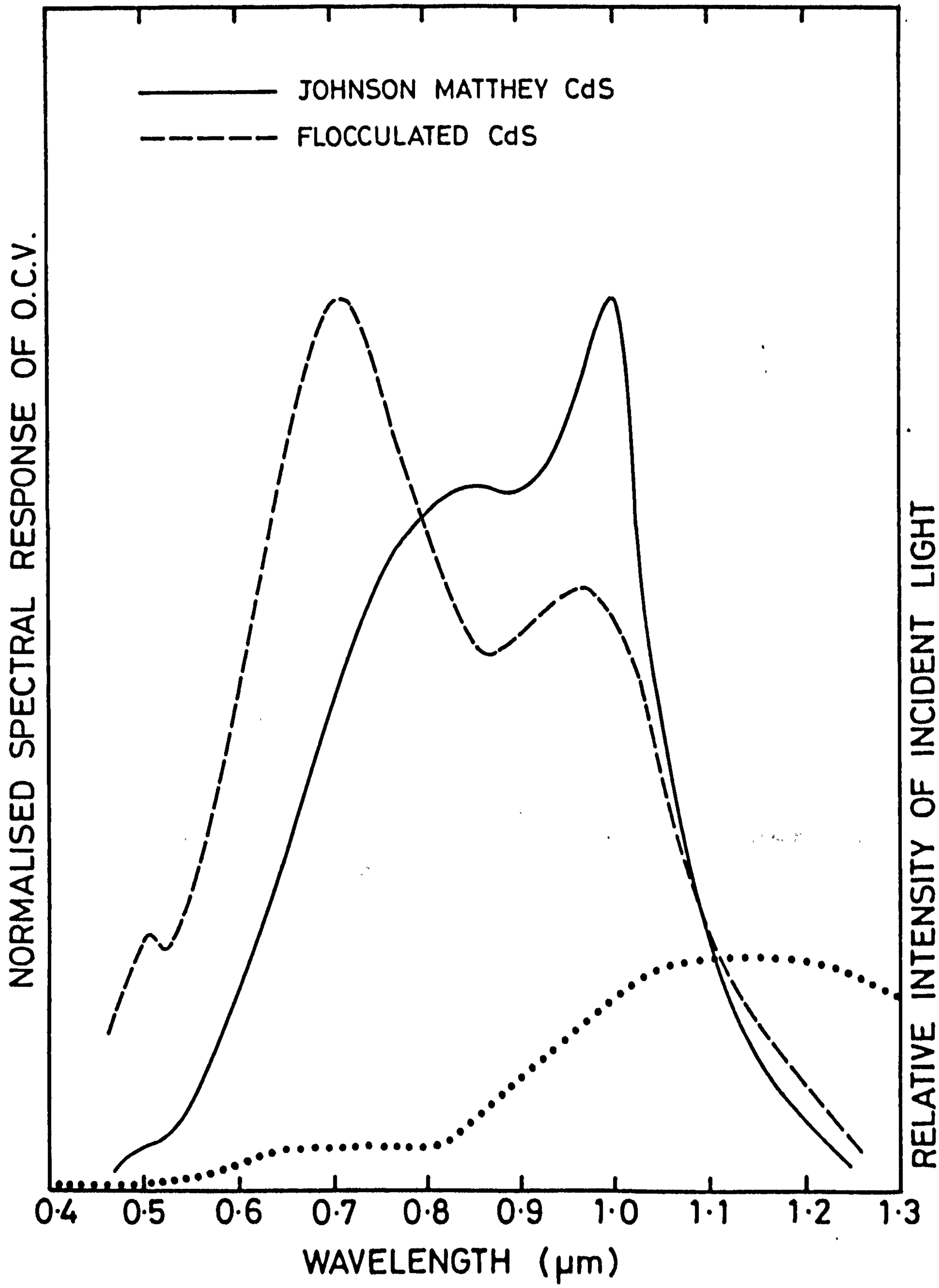


FIGURE 7.17: Spectral responses of the OCV of heterojunctions formed on films prepared from different sources of CdS.

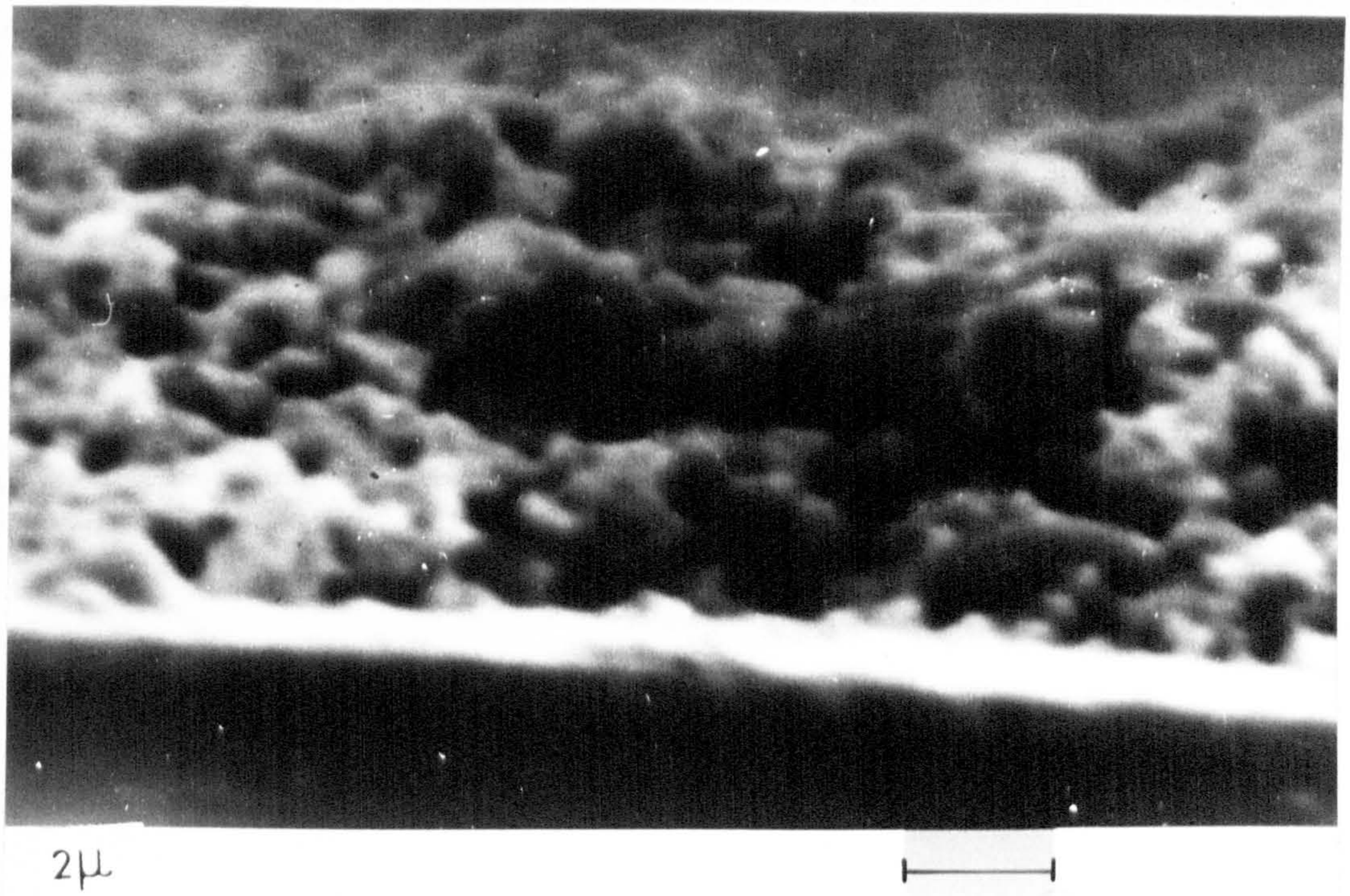


FIGURE 7.18: S.E. micrograph of an as-prepared film deposited with PVP

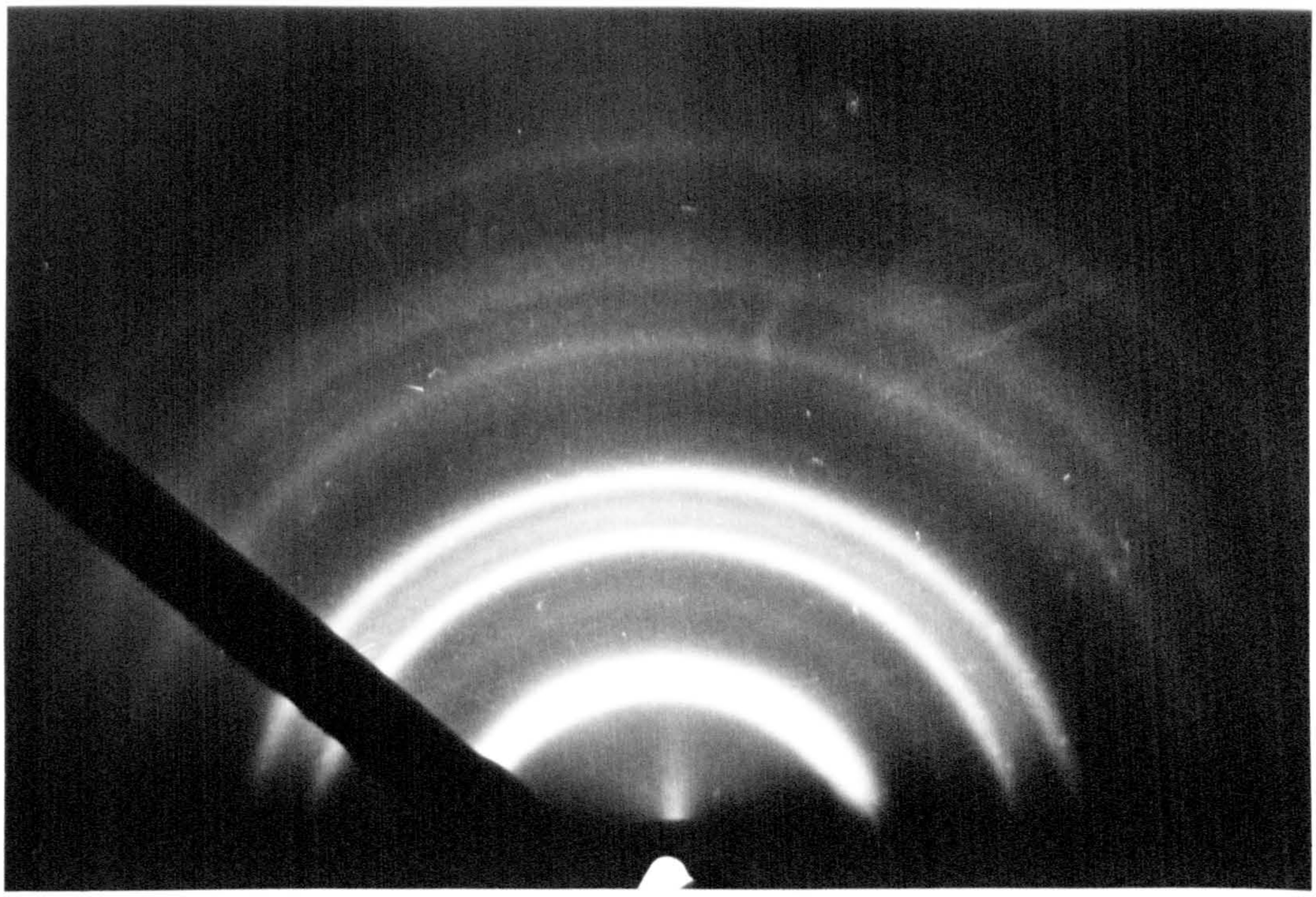


FIGURE 7.19: RHEED pattern for the above film

TABLE 7.5: Effect of Different Treatments on the Resistivities of the Thicker Films

(a) Indium doping		(b) Temperature of Annealing	
Indium Concentration (mol %)	Resistivity* (k Ω-cm)	Temperature and duration of treatment	Resistivity** (k Ω- cm)
Nil	10	530 for 10 min	500
0.001	3	530 for 10 min	300
0.01	1.8	550 for 10 min	220
0.1	1.0	600 for 10 min	5
0.13	0.5	640 for 10 min	0.5

* After annealing in argon at 640^{o}C for 10 minutes.

** for film containing 0.13 mol % In.

These results show that the resistivity can be reduced by increasing either the In concentration or the annealing temperature. It is worth pointing out that the considerable reduction in the resistivity that can be achieved by annealing at temperatures of 600^{o}C and above is possible with thicker films. The RHEED pattern after heating at 600^{o}C for 20 min is shown in Fig 7.20, and indicates that, in addition to phase conversion, there is grain growth as evidenced by the spottier nature of the diffraction rings. This suggestion is supported by the scanning electron micrograph of the cross section of this film which indicates that the particle size is much larger following the 600^{o}C anneal (Figure 7.21).

The uncompensated donor density for a film containing 0.01% mol In annealed at 640^{o}C for 10 min was found to be 4.6 x 10^{15} cm^{-3} with a mobility

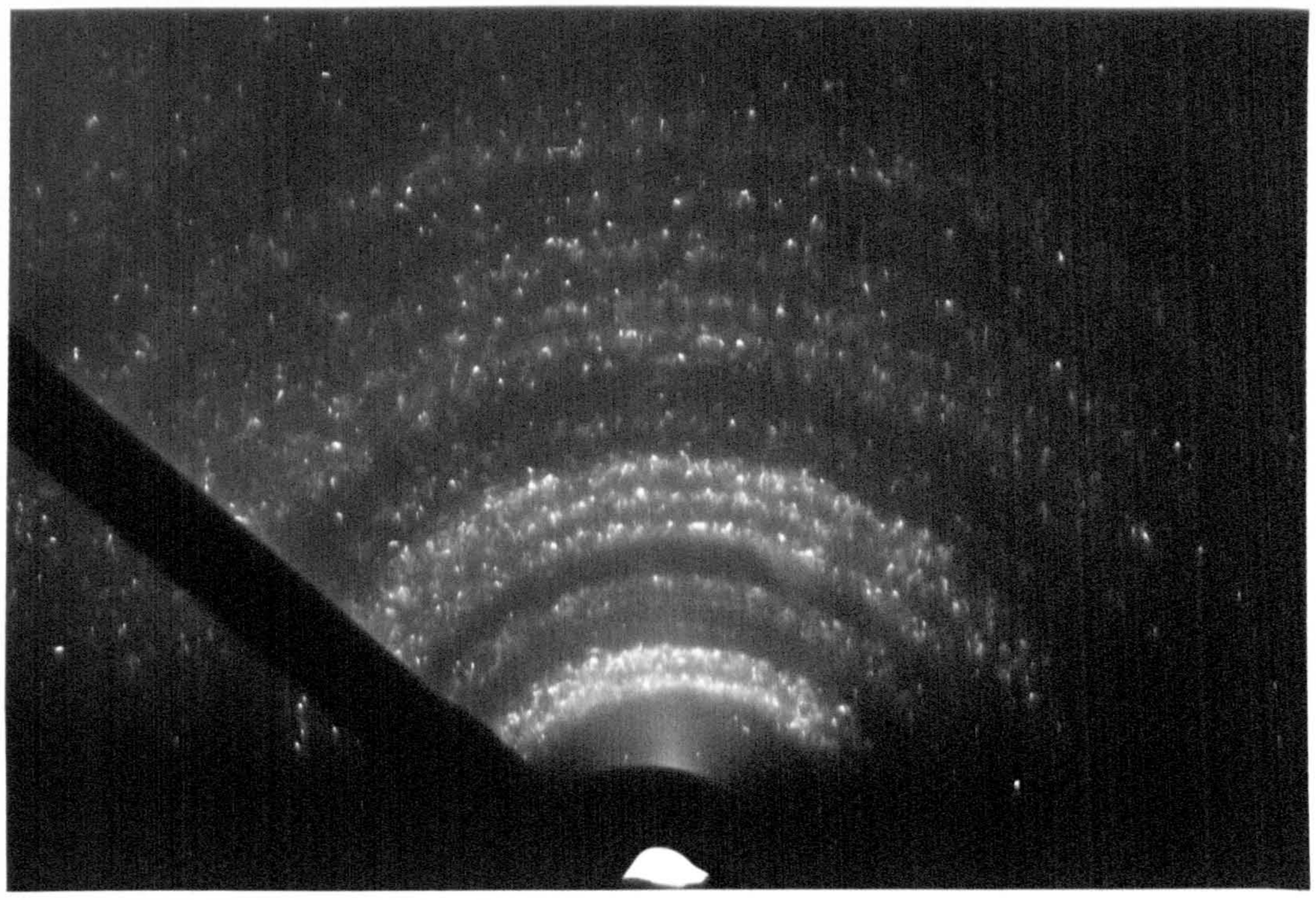


FIGURE 7.20: RHEED pattern for the film (Fig 7.19) after the deposition of a $CdCl_2$ overlayer and heating at $600^{o}C$ for 20 min

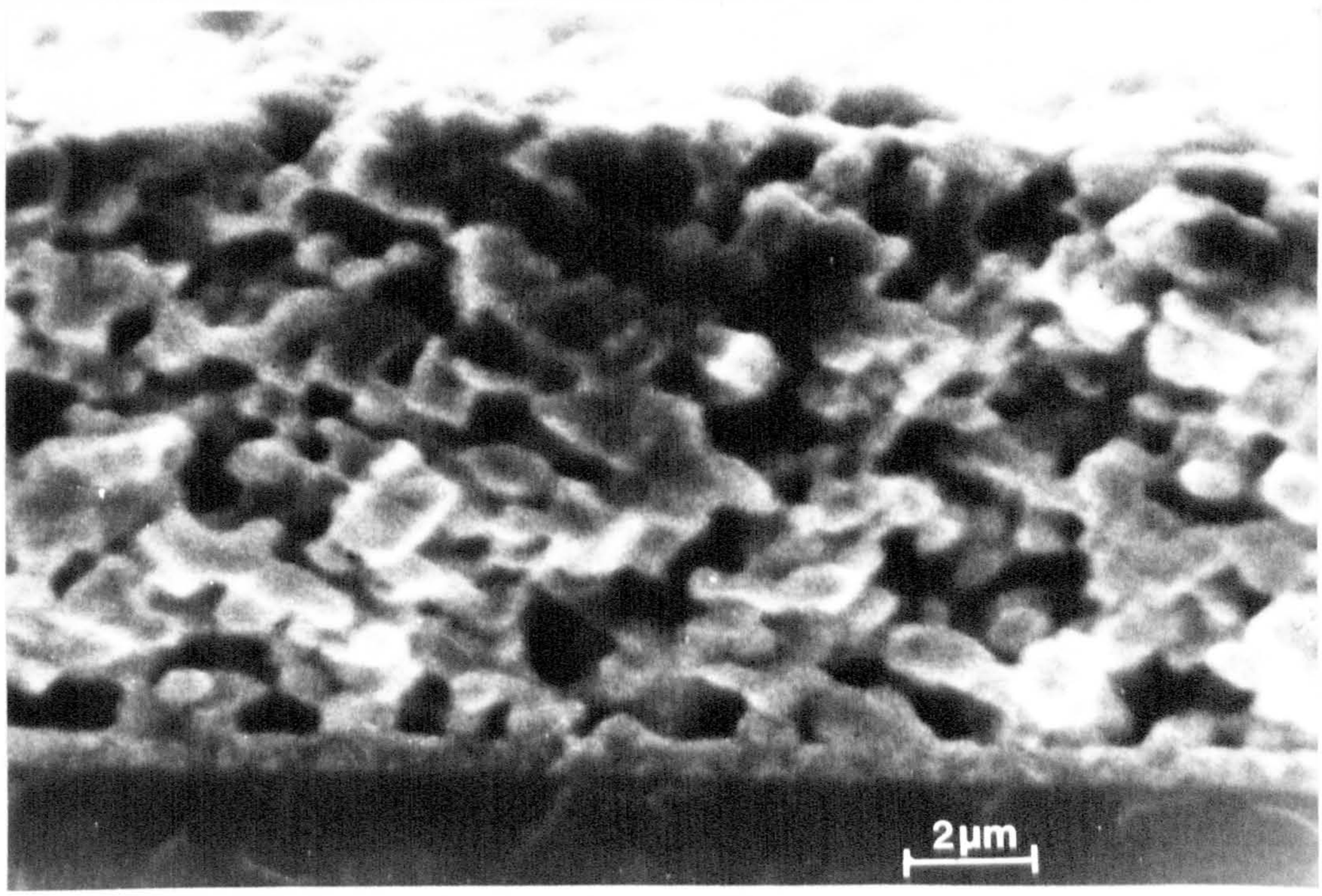


FIGURE 7.21: S.E. micrograph of the above film

of 1.3 $cm^2\ V^{-1}\ s^{-1}$. In general it was found that the measured mobility values varied from 1 to 5 $cm^2\ V^{-1}\ s^{-1}$ with different samples, where the intergranular barrier height was found to be about 0.18 eV. Finally it is worth noting that the films became mechanically harder after $CdCl_2$ treatment.

7.7.2 Device Characteristics

Heterojunctions were prepared on the In doped (0.13 % mol) thicker CdS films treated with $CdCl_2$ and annealed at 640°C for 10 min. For this a layer of 0.15 μm CuCl was vacuum deposited on to the films and a heat treatment of 2 min at 200°C in argon was given to form the junction. The resultant J-V characteristics are shown in Fig 7.22. In general it was found that the SCCs obtained from devices on these films were about four times larger than those obtained from the devices formed on the films prepared from flocculated CdS. This is certainly due to their lower resistivity. The OCV was about 0.4V.

A typical spectral response of the OCV of a heterojunction formed on one of the In doped film is shown in Fig 7.23. The predominant peak near 0.98 μm indicates that chalcocite is largely responsible for the response of the cell. This clearly demonstrates that introducing indium into these electrophoretically deposited CdS films does not adversely affect the formation of this desired phase of Cu_xS.

7.8 DISCUSSION

The reflection electron diffraction studies show that the as-deposited electrophoretic layers of CdS had the sphalerite cubic phase. Annealing the layers in argon at progressively higher temperatures led to an increasing proportion of the wurtzite, hexagonal phase. When over-layers of $CdCl_2$ were used, the conversion to wurtzite occurred at a substantially lower temperature, so that heating at 450°C for 30 min led to films with a greater wurtzite content than those annealed for 10 min at 530°C in the absence of $CdCl_2$. This latter treatment was the maximum anneal which could be administered to

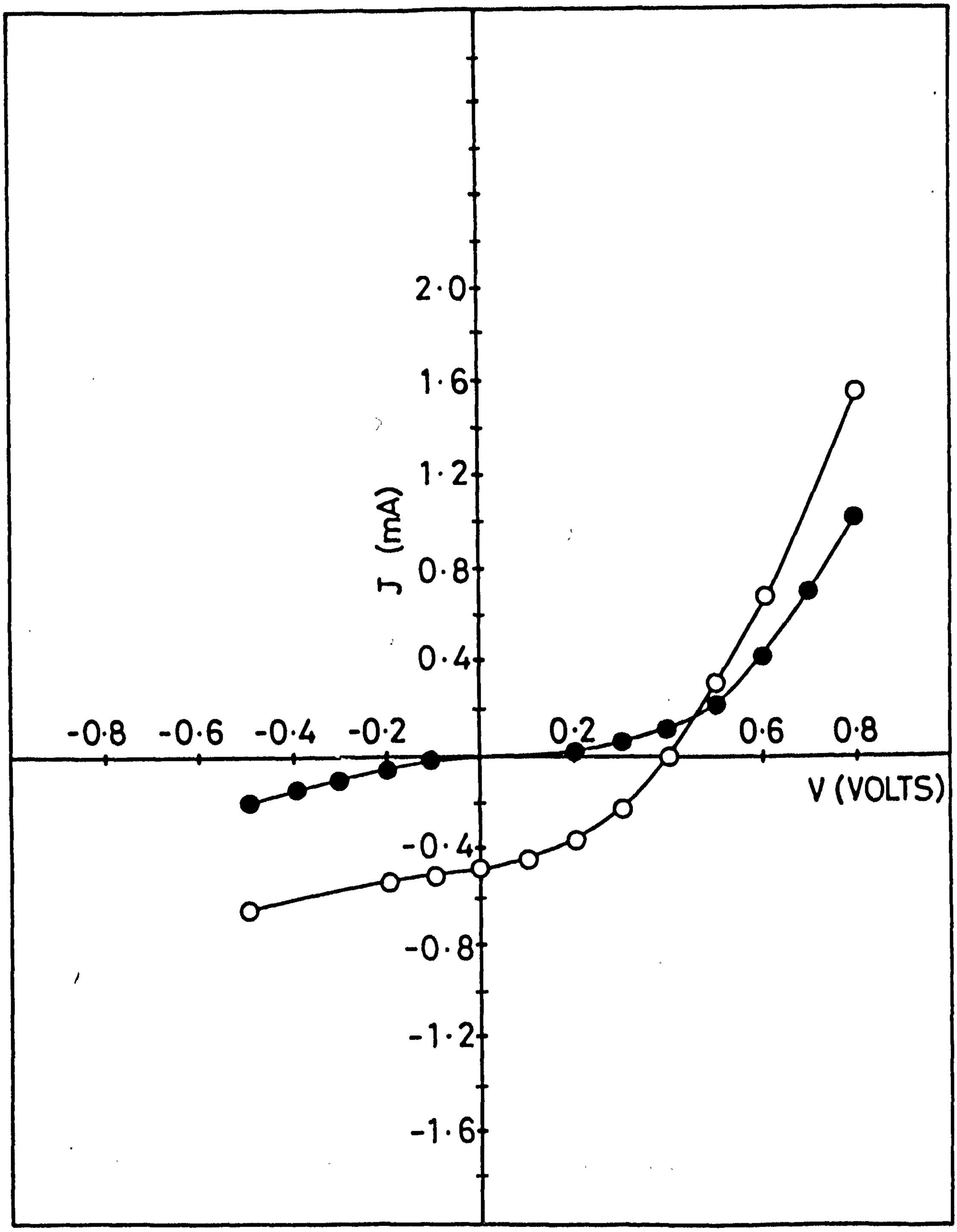


FIGURE 7.22: J-V characteristics of a heterojunction formed on an indium doped thicker film of CdS deposited by electrophoresis with PVP as binder

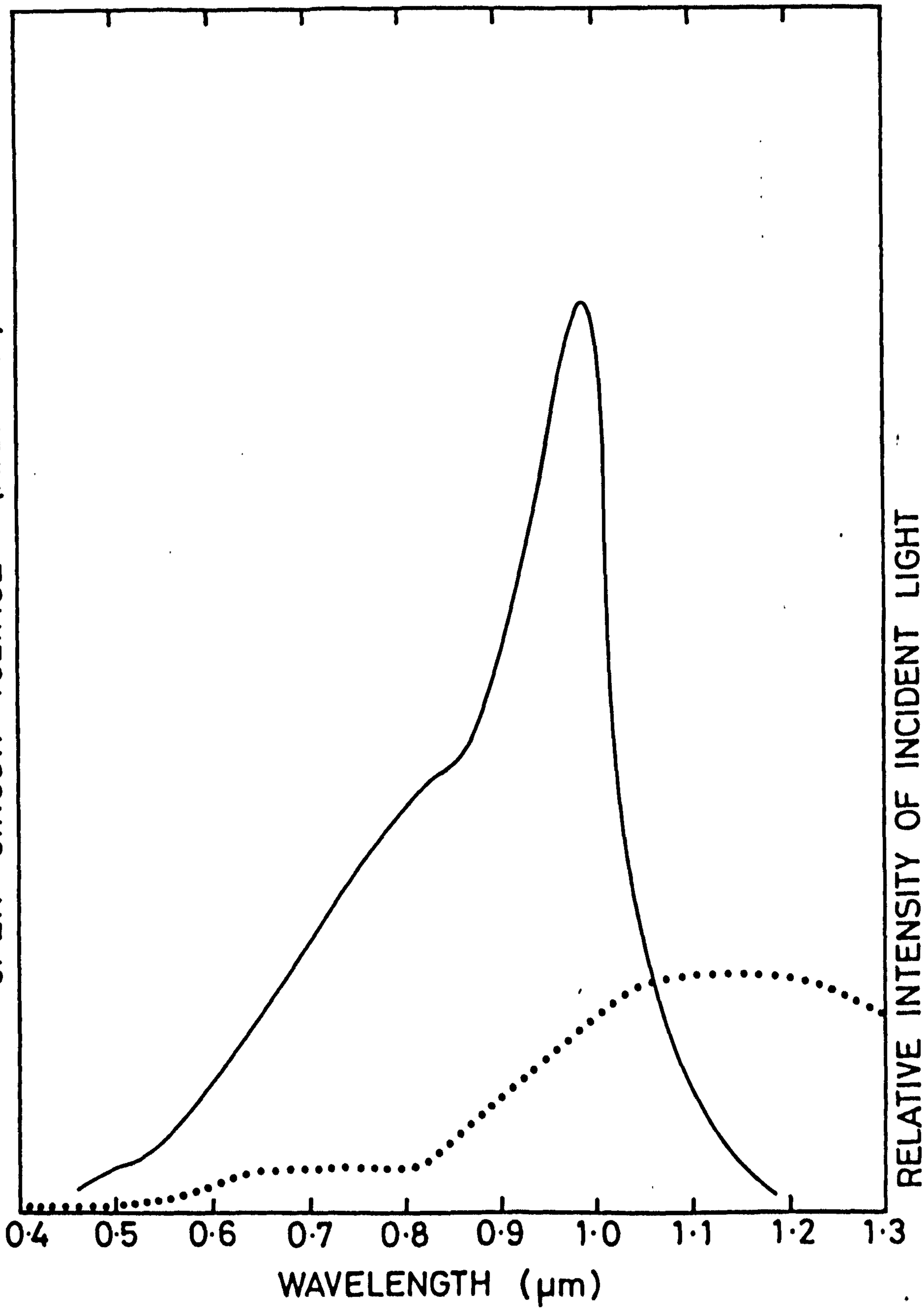


FIGURE 7.23: Spectral response of the OCV of the heterojunction formed on an indium doped CdS film deposited by electrophoresis with PVP as binder

binderless (~ 2 μm) films before pin holes developed. Thicker films with PVP binder could be subjected to higher temperatures and when $CdCl_2$ was present, significant grain growth took place at 600°C. These observations may be related to the findings of many workers who observed a lowering in the recrystallization temperature either by doping with group 1-B elements such as Ag or Cu[25-30] or annealing in H_2S[31,32]. However, these treatments led to resistive films which were not suitable for photovoltaic application. In the absence of such dopants a much higher temperature is required (>700°C) to promote grain growth[30]. This temperature is too high for films deposited on glass substrate because the glass softens and the CdS tends to evaporate. In this context the effect of $CdCl_2$ in these films is significant as it assists the recrystallization and simultaneously reduces the resistivity of the film[33].

The results in Tables 7.2 and 7.3 show that the electrical resistivity of films treated with $CdCl_2$ could be reduced by some 4 orders of magnitude by appropriate annealing, whereas the resistivity of untreated films could only be reduced by about 2 orders. The uncompensated donor density increased with annealing temperature and was generally larger when $CdCl_2$ was used. The effect of the chloride was more pronounced at the lower annealing temperatures. It is interesting to note that the highest donor concentrations were close to 10^{16} cm^{-3}. Such a donor concentration in a single crystal would have led to a resistivity of approximately 5 ohm-cm, which would be near to optimum for an efficient Cu_2S-CdS solar cell. The fact that the resistivity of the thin films could not be reduced below 6×10^2 ohm cm by annealing is attributable to the presence of potential barriers at the intergranular boundaries. According to Volger[34] the mobility, μ, of a polycrystalline layer limited by intergranular barriers of height ϕ eV is

$$\mu = \mu_o \exp(-e\phi/kT)$$

where $\mu_o = elv_{th}/4\beta kT$, in which l is the dimension of a grain, v_{th} is the

thermal velocity of the electrons and β is a numerical constant which has a value of 8.0 for back to back Schottky barriers. Assuming a grain size of 400 Å leads to values of barrier height near 0.14 eV when the annealing is done in the presence of chlorine, and 0.18 eV when untreated layers are annealed. The presence of the chlorine therefore increases the donor concentrations, which decreases the barrier height slightly. When similar calculations were carried out for the thicker films, prepared with PVP binder, barrier heights of 0.18 eV were then found, even when $CdCl_2$ was used. However mobilities were higher in the range 1-5 $cm^2\ V^{-1}\ s^{-1}$ reflecting the increased grain size and consequent reduction in the number of inter-particle boundaries. The increased barrier height in the presence of the binder appears to be a function of a reduction in the packing density of the layer. With the phase transformation the colour of the films changed from dark yellow to buff yellow. The difference in the absorption edge between the cubic and hexagonal CdS is expected to lead to such a change in colour[35]. In addition to this, the mechanical properties were also found to improve after $CdCl_2$ treatment. Though no quantitative assessment was performed, the film was resistant to brushing in contrast to its very soft texture in the as-made condition. The effect of $CdCl_2$ on the mechanical properties of the electrophoretically deposited film has been reported by Ueno et al[4], when $CdCl_2$ was used in the plating bath. In the thermal evaporation method $CdCl_2$ was also found to provide better adhesion to CdS films on to glass substrate[36]. Moreoever, in the vapour phase growth of CdS single crystals in this laboratory the presence of chlorine has been found to promote a glossy appearance as if the surface has melted. These observations suggest that the presence of chlorine tends to promote increased surface mobility which would activate the recrystallisation.

In addition to these effects of the $CdCl_2$ treatment on the structure of the film, the photocapacitance studies suggest (see section 7.5) that besides introducing shallow donors, substitutional chlorine is associated with a deeper

donor with an ionization energy of 0.28 eV. Acceptor levels, 1.0 eV above the valence band are also introduced at the same time which are probably the acceptor components of the self-activated luminescence emission centre.

The heterojunction formed on the $CdCl_2$ treated thin films (without binder) gave a dominant peak in the spectral response of the OCV at 0.62 μm which can be attributed to the copper centres in CdS[19]. Since these devices were formed with a thin layer (600 Å) of CuCl, the main response arises from these centres[20].

The area of the device was restricted by a 1.4 mm dot of CuCl to avoid any short circuiting. With the thicker films the area of the device as well as the thickness of the Cu_xS layer could be increased. The spectral response of the devices on the thicker films was found to depend on the source of CdS powder used. Devices on the films prepared from flocculated CdS had a major response at 0.7 μm which can be attributed to remnants of chlorine and unconverted cubic CdS which might be present in the film affecting the phase of Cu_xS adversely[37]. Since the Johnson Matthey material was hexagonal under as-prepared conditions the enhanced response at 0.96 μm reflects the domination of chalcocite phase. The presence of the other peak at 0.78 μm reflects the djurleite content which can be attributed to the adverse effects of residual chlorine[37]. The lower values of SCC can be attributed to the higher resistivities of these films. On the less resistive films prepared from indium doped powder the device gave a predominant response at 0.98 μm and the SCC was four times larger than that obtained from flocculated CdS. Although the use of indium proved advantageous with electrophoretic devices this improvement was not consistent with the results obtained using screen printed layers of indium doped CdS (see Chapter 8), where indium had a deleterious effect on the device parameters.

7.9 CONCLUSIONS

It has been demonstrated that heating electrophoretically deposited films of CdS carrying overlayers of $CdCl_2$ can have considerable effects on

their electrical and structural properties. As deposited, the films are cubic with a very small grain size. Heating in argon promotes a transition to hexagonal phase which is virtually complete at 450°C when $CdCl_2$ is present. Significant grain growth does not take place until the temperature is raised to 600°C, but for this to occur it is necessary to use a much thicker layer of CdS, or material loss will lead to the break up or disappearnace of the layer. Successful deposition of such thick layers has only been accomplished when a binder was added to the sol. Grain growth in the presence of $CdCl_2$ has also been reported by Millikov and Khiie[38] and Matsumoto et al[39] have commented on the enhancement of phase changes in CdS powder in the presence of NaCl.

The use of $CdCl_2$ with the electrophoretic layers of CdS has led to the incorporation of shallow donors so that resistivities as low as 6×10^2 Ω-cm can be achieved. This corresponds to an uncompensated donor concentration of 2.7×10^{16} cm^{-3} and a mobility of 0.38 $cm^2 V^{-1} s^{-1}$. The low values of the mobility are caused by the potential barriers at the intergranular boundaries. These barriers are between 0.14 and 0.18 eV high, depending on the chlorine concentration.

Photocapacitance studies are interpreted to suggest that transitions from filled levels to the conduction band are associated with cadmium vacancies and alkali metal impurities, whereas transitions from the valence band to empty levels were also observed in the presence of chlorine, and these are assigned (1) to the defect complex of a cadmium vacancy and neighbouring chlorine impurity as with the activator of the well known self-activated luminescence, and (2) to a second deeper donor level of substitutional chlorine.

Heterojunctions were formed on these $CdCl_2$ treated films by the dry barrier process. The spectral response of the devices showed that chalcocite layers of Cu_xS could be prepared on these films. The OCV was $\tilde{\sim}$ 0.4 V while the short circuit current was found to be limited by the resistivity of the films. With the lowering of the resistivity the SCC could be increased by a

factor of four. Even then the values of the SCC (3.4 mA/cm^2) were limited by the effects of the inter granular boundaries[40].

REFERENCES TO CHAPTER 7

1. E.W.Williams, K.Jones, A.J.Griffiths, D.J.Roughley, J.M.Bell, J.H.Steven and M.J.Huson, M.Rhodes and T.Costich, Solar Cells,(1979/80), 1, p.357.

2. - ibid Proc. Spec. Photovoltaic Conf., Berlin,(1979),p.874,

3. W.R.Cook, L.R.Shiozawa and F.Augustine, J.Appl.Phys, 41,(1970)p.3058.

4. Y. Ueno, H.Minoura, T.Nishikawa and M.Tsuiki, J.Electrochem.Soc. 130 (1983), p.43.

5. J.C.Shaefer, R.J.Humrick . E.R.Hill and R.F.Belt, Final Rep. ASD-TDR-63-743, Harshaw Chem.co.1963.

6. S.D. Sathye and A.P.B.Sinha, Thin Solid Films 37, (1976), p.15.

7. W.O.Milligan, J.Phys.Chem.38 (1934) p.797.

8. E.S.Rittner and J.H.Schulman, J.Phys.Chem.47, (1943), p.537.

9. K.V.Shalimova, A.F.Andrushko, V.A.Dmitriev and L.P.Pavlov, Soviet Phys.Crystallography 8(1964), p.618.

10. R.R.Chamberlin and J.S.Skarman, J.Electrochem.Soc, 113 (1966), p.86.

11. Y.Y.Ma and R.H.Bube, J.Electrochem.Soc. 124, (1977), p.1430.

12. E.H.Rhoderick, Metal Semicond.Contacts, Clarendon Press,Oxford, (1980).

13. R.H.Bube, Electron Properties of Crystalline Solid, An Introduction to Fundamental Academic Press, (1974), p. 310.

14. C.M.Henry, K.Nassan and J.W.Shiever, Phys.Rev. B5, (1972), p.458.

15. J.Woods and D.A.Wright, Solid State Physics in Electronics and Telecom. Proc.Int.Conf.Brussels, (1958), p.820.

16. A.Qidwai and J.Woods, J.Phys.C: Sol. St.Phys.16, (1983), p.6787.

17. Y.Marfaing, J.Lascaray and R.Triboulet, Metal Semiconductor Contacts, Inst.of Phys.Conf.Series, 22, (1979), p.201.

18. T.J.Cumberbatch, I.D.McInally, E.W.Williams, D.J.Gibbons, M.Claybourn, H.Clow and P.M.G.Dickinson, R.Hill, N.M.Pearsall, J.Woods, G.Russell and P.C.Pande, Proc.4th E.C.P.V.Solar Energy Conf. (D.Reidel:London) (1982), p.551.

19. B.G.Caswell, G.J.Russell and J.Woods, J.Phys.D.8 (1975), p.1889.

20. P.C.Pande, G.J.Russell and J.Woods, Proc.5th E.E.C. P.V.Solar Energy Conf., Athens, Greece, (1983), p.171.

21. G.J.Russell, P.C.Pande, J.Woods, I.D.McInally and S.P.Gibbons, Inst.Phys.Conf.Ser. No.67, (1983), p.189.

22. T.H.Weng, J.Electrochem.Soc. 126, (1979), p.1820.

23. E.D.Jones and H.Mykura, J.Phys.Chem.Solids, 39 (1978), p.11

24. G.J.Russell, P.C.Pande, A.E.Thomas, J.Woods, T.J.Cumberbatch, I.D.McInally and L.Holt, Proc.5th E.E.C.Photovoltaic Solar Energy Conf., Athens, Greece (1983), p.855.

25. J.M.Gilles and J.Van Cakenberghe, Nature 182, (1958), p.862.

26. J.Dresner and F.Shallcross, J.Appl.Phys. 34, (1963), p.2390.

27. R.R.Addiss, In Trans.X.Nat.Vacuum Symp, MacMillan Co.New York, (1963), p.354.

28. A.Vecht and A.Apling, Phys.Stat.Sol.3, (1963), p.1238.

29. C.Herinchx, W.Deshutter, A.Fourdeux and N.Terao, Phys.Stat.Sol.(a), 10, (1972), p.387.

30. W.Kahle and H.Berger, Phys.Stat.Sol.(a), 2, (1970), p.717.

31. L.M.Frass, W.P.Bleha and P.Braatz, J.Appl.Phys, 46, (1975), p.491.

32. R.S. Srivastava and K.Prakash, J.Appl.Phys. 50, (1977) p.7245.

33. P.C.Pande, G.J.Russell, J.Woods, To be published in Thin Solid Films.

34. J.Volger, Phys.Rev. 79, (1950), p.1023.

35. M. Bujjatti, Phys.Letters 24, (1967), p.36.

36. R.Hill, In Active and Passive Films, Ed. T.J.coutts, Academic Press, London, (1978). p.487.

37. W.Palz, J.Besson, T. Nguyen Duy and J.Vedel, Proc.9th IEEE Photovoltaic Specialists Conf., (1972), p.91.

38. E.Ya. Millikov and Ya. V.Khiic, Inorganic Materials, 17, (1981), p.1164.

39. K. Matsumoto, K.Takagi and S. Kaneko J.Electrochem Soc.130, (1983), p.423.

40. L.M.Frass, J.Appl.Phys. 49 (1978), p.871.

CHAPTER 8

HETEROJUNCTIONS FORMED ON SILK SCREEN PRINTED FILMS

8.1 INTRODUCTION

In view of the problems of the limiting thickness and high resistivity of the electrophoretically deposited films of CdS, a study was carried out concurrently on silk screen printed layers of the same batches of CdS starting materials which were used for the electrophoretic deposition. An initial study was made to establish suitable preparative parameters for silk screen printing, such as particle size, quantity of flux, type and quantity of binder, sintering temperature etc. In addition, the effect of indium on the conductivity of the layers was thoroughly investigated and heterojunctions were formed by the dry barrier process on undoped layers, as well as on those doped with various concentrations of indium. Current-voltage characteristics, spectral response and steady state photocapacitance measurements were carried out to determine the effect of indium on the device characteristics.

A few attempts were also made to prepare films of indium doped $Cd_{1-y}Zn_yS$.

8.2 MATERIAL ASPECTS

8.2.1 Preparation of Phosphors

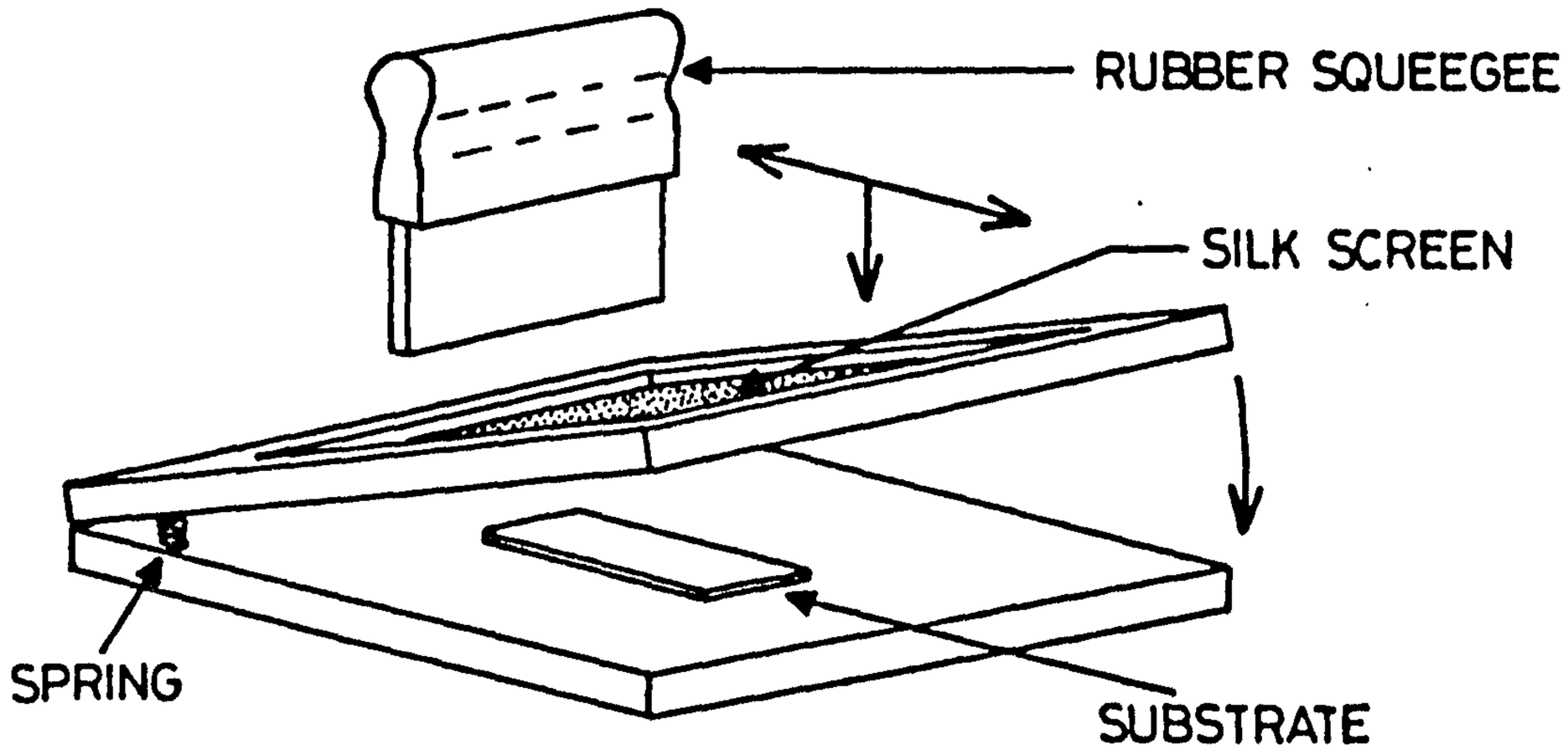
Commercially available cadmium sulphide (optran grade) was mostly used in this study. The as-received powder (grain size $\tilde{>}$ 40 μm) was ground for 2 min in a TEMA swing mill. The resulting CdS powder was then made into an aqueous paste with 6% (by weight) of CdF_2. This particular fluoride was chosen with a view to introducing donors and increasing the surface potential of the particles. When doping with indium was employed, the required quantity was added to the paste in the form of $InCl_3$. The paste was then dried at 100°C with continual stirring to ensure that the CdF_2 and

$InCl_3$ was distributed as uniformly as possible. The dried powder was placed in a silica capsule, and after being compacted was held in position by another closed silica tube of slightly narrower bore. This arrangement was then inserted in an open ended silica tube which was placed inside the furnace, through which a continuous flow of argon was passed. The powders were fired for 2 hours at 850° C after which they were cooled at the entrance to the furnace, while the flow of argon was maintained. The cake of CdS formed in this way was swing milled for different periods ranging from 2-15 min in order to produce powders with different particle sizes. To prepare solid solutions of $Cd_{1-y}Zn_yS$, commercially supplied CdS and ZnS were mixed in the appropriate proportions. The mixture was ground in the swing mill for 15 min. As before, an aqueous paste was prepared with water to which measured quantities of CdF_2 and $InCl_3$ had already been dissolved, and the same procedure was followed as with the CdS powders.

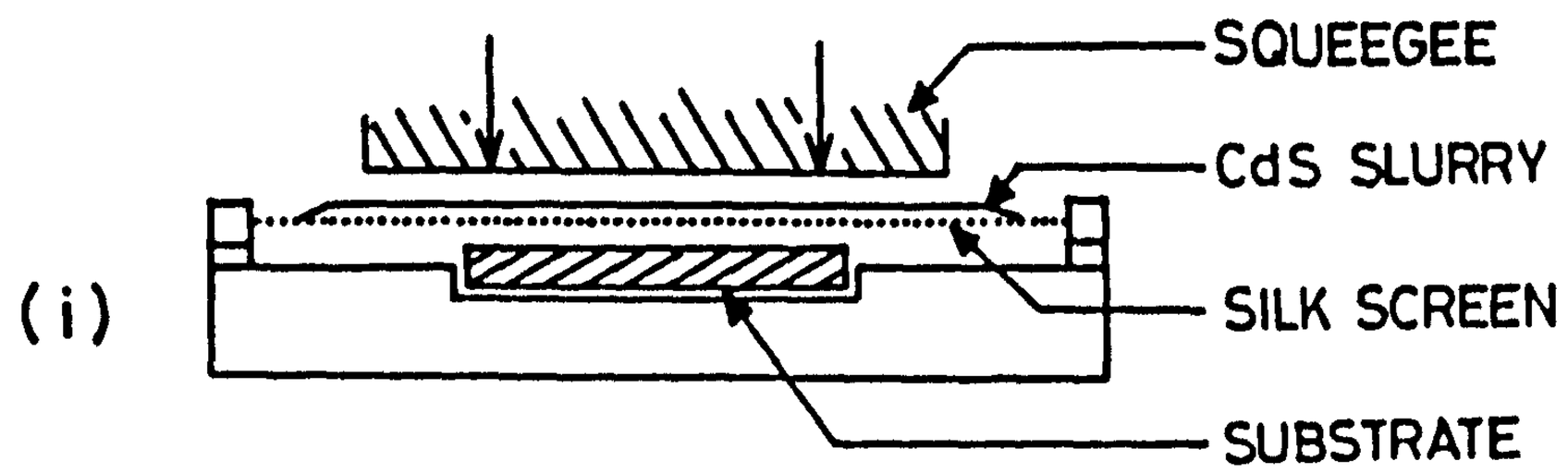
8.2.2 Silk Screen Printing

For the silk screen printing, propylene glycol and $CdCl_2$ were used as binder and flux. The quantity of $CdCl_2$ varied between 6 to 30%, and that of the propylene glycol between 25 to 35%. The $CdCl_2$ was first dissolved in the propylene glycol by ultrasonic stirring and this solution was used to make the slurry of CdS. In general it was found that the most effective procedure was to use 28% of propylene glycol to make the slurry and then add a few more drops until the mixture became thixotropic which is essential if a uniform spread of the film is to be achieved[2]. If the slurry is too stiff it is difficult to spread and screen marks appear on the film, while if it is too liquid, the spread becomes patchy. With the solid solutions of $Cd_{1-y}Zn_yS$, a mixture of $CdCl_2$ and $ZnBr_2$ was also investigated as a flux.

The equipment used for spreading the films was of a very basic design (Fig.8.1). It consisted of a wooden frame on which the silk screen (120 μm mesh) was tightly stretched and fixed. Films were deposited on conventional



SILK SCREEN PRINTER



SILK SCREEN PRINTING SEQUENCE

FIGURE 8.1: A schematic diagram of the equipment and illustration of the silk screen printing process of CdS layers

glass microscope slides as well as on conducting glass substrates. The substrates were thoroughly cleaned using 5% Decon-90 solution followed by rinsing first with deionized water and then isopropyl alcohol. The substrates were then kept in isopropyl alcohol vapour until they were required. For silk screen printing, the cleaned substrates were confined within a recess provided on the base of the printing equipment and were then covered by the silk screen. The slurry was poured onto the screen and spread over the glass substrate as evenly as possible using a rubber squeegee. Two springs located at the end of the wooden frame provided the necessary upthrust while removing the silk screen. The films were oven-dried for four hours at 120°C. The 20-30 μm thick films were then fired for varying periods at different temperatures ranging from 600 to 700°C. In order to anneal films in cadmium vapour, a piece of Cd metal (∿ 5 gm) was placed in the open silica tube together with the CdS layers being heat treated. Finally ohmic contacts were provided to these films by indium so that measurements of the sheet resistance or resistivity of the films could be made.

8.3 RESULTS

8.3.1 Electrical and Structural Properties of Sintered Films

In general it was found that the firing in the presence of Cd vapours reduced the sheet resistance of the films by an additional order of magnitude. The quantity of $CdCl_2$ required as a flux to produce a well sintered film was found to vary with the particle size of the powder. The samples swing milled for 2 and 15 minutes required 10% and 20% of $CdCl_2$ respectively. Further, the temperature and duration of sintering both affected the structure and resistivity of the films. The measured values of sheet resistance ($R_\square$) of sintered films prepared from powders swing milled for different lengths of time are summarized graphically in Fig 8.2, which illustrates a few important trends. For example, as the temperature of sintering was increased from

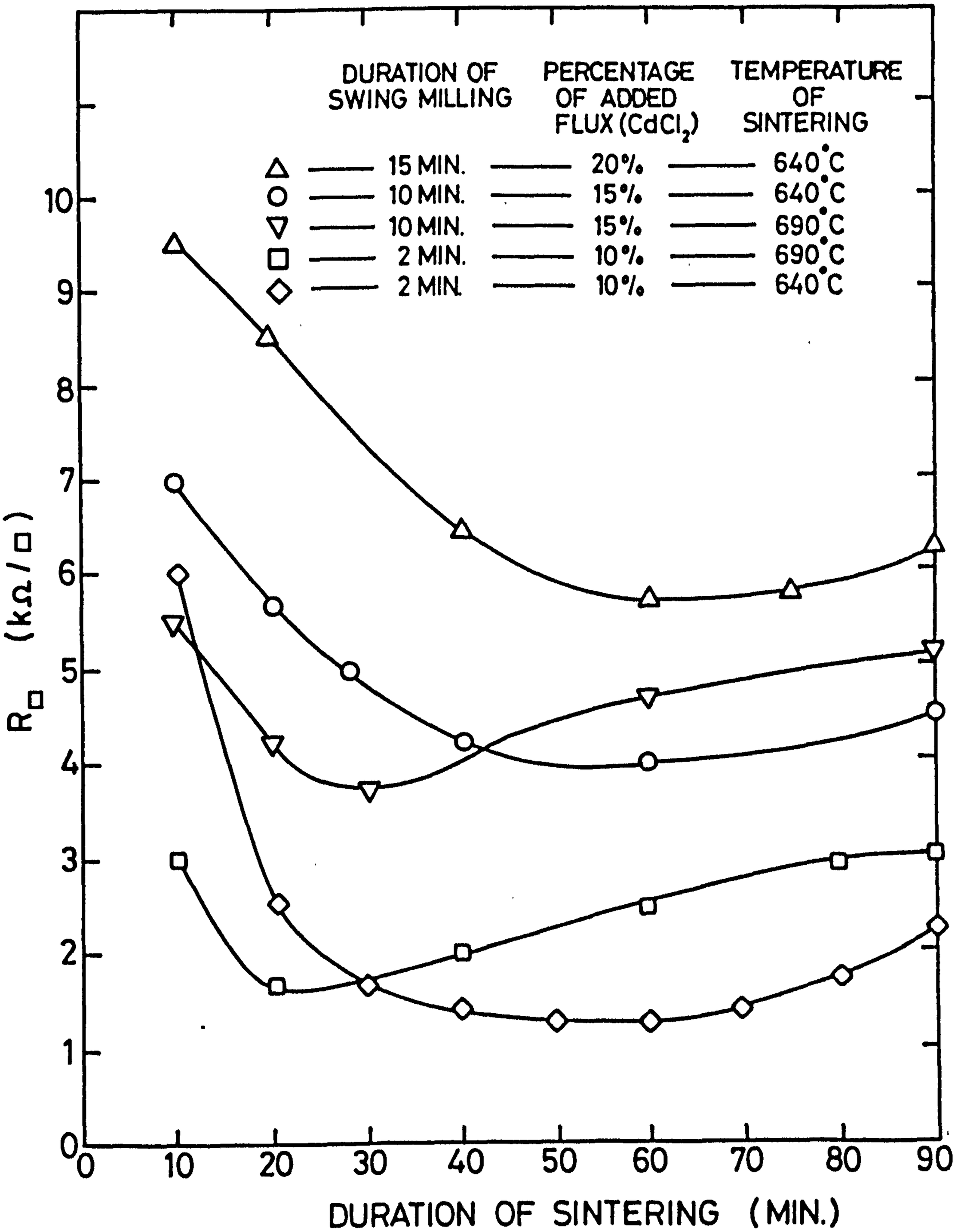


FIGURE 8.2: Variation of the sheet resistance of silk screen printed films prepared from CdS powders swing milled for different lengths of time.

640 to 690°C the films required a shorter sintering period to develop the minimum resistance. Thus at 640°C the films had to be sintered for ≃ 60 min while 20 min only was required at 690°C. Those powders which were swing milled for the shorter periods yielded lower values of sheet resistance and these were obtained after shorter sintering periods. Thus the minimum value of $R_{\square}$ which was obtained for the films prepared from powders swing milled for 10 min were about three times larger than those of films prepared from powder swing milled for 2 min. The sheet resistance increased slightly when these films were heated for longer than 30 min at 690°C or 60 min at 640°C. Finally the curve corresponding to films prepared from powder swing milled for 15 min shows that such treatment led to high resistances for all the powders studied.

The sharp reduction in the resistance for annealing periods of 10-20 mins can be attributed to the combined processes of sintering, loss of sulphur and introduction of shallow donors by chlorine. The overall result seemed to be affected by the particle size, since the powder swing milled for longer times led to more resistive films.

Although resistance values are quoted for films annealed at 690°C, the glass substrates softened and bent at this temperature and as a result most films were sintered at 640°C for 60 min. A scanning electron micrograph of a film treated in this way is shown in Fig.8.3a which reveals a smooth texture suggesting that the surface has undergone a "melting process". However some grain boundaries still existed and these become more obvious when the same region was observed in the absorbed current mode of operation of the SEM (Fig 8.3b).

The effect on the resistance of the layers of varying the indium concentration is demonstrated by the results in Table 8.1.

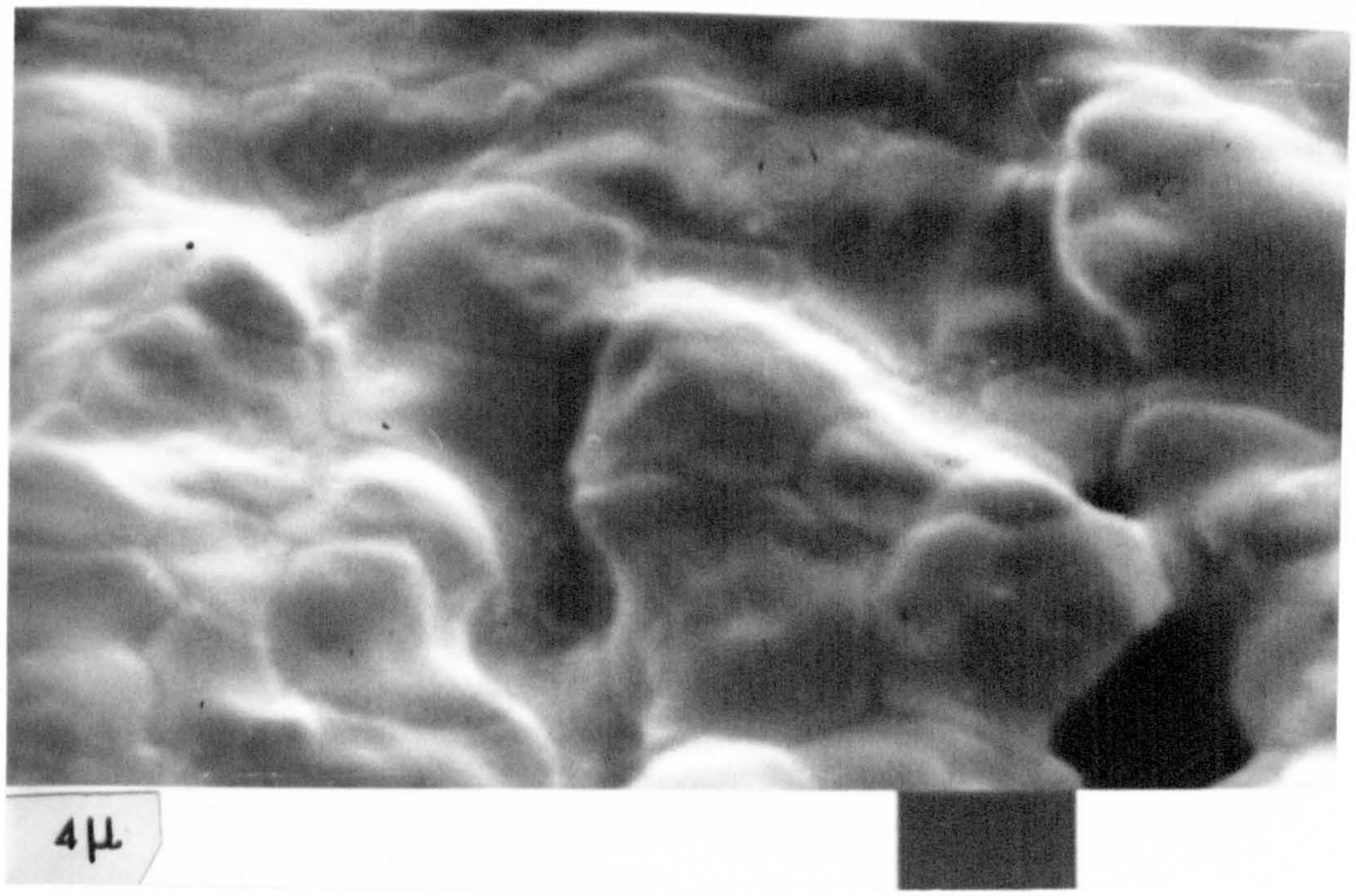


FIGURE 8.3(a): S.E. micrograph of a silk screen printed sintered CdS film

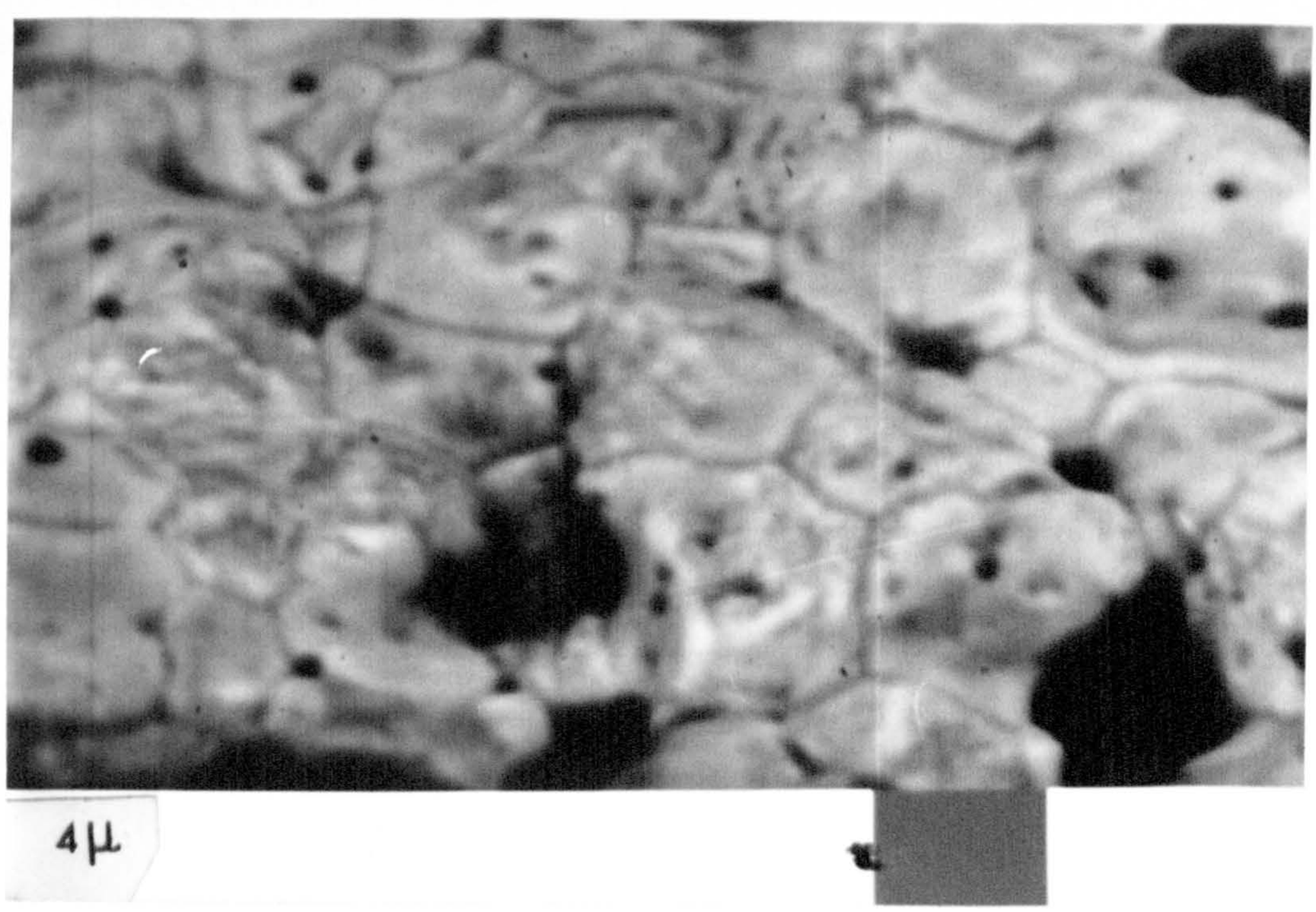


FIGURE 8.3(b): S.E.micrograph in absorbed current mode of the film shown above in Fig 8.3(a).

TABLE 8.1: The effect of Indium Concentration on the Sheet Resistance of Sintered CdS Films.

Mol % of In doped in the CdS	SHEET RESISTANCE OF FILMS PREPARED FROM CdS POWDER (KΩ/□)			
	Swing Milled for 10 mins and sintered at 640° for 60 min		Swing Milled for 2 mins and sintered at 640°C for 60 min	
	With Cd vapour	Without Cd vapour	With Cd vapour	Without Cd vapour
0	4	35	1.25	10
0.001	3	30	0.48	3
0.01	1.25	14	0.1	0.9
0.1	0.65	10	0.1	0.9
0.5	2	25	1.1	8

With the more conducting films prepared by sintering in cadmium vapour, Table 8.1 indicates that the sheet resistance decreased from 1.25 to 0.1 KΩ/□ as the indium content was increased to 0.1% mol using powder swing milled for 2 min. With powder swing milled for 10 min the corresponding reduction in resistance was from 4.0 to 0.65 KΩ/□. However on increasing the indium content further to 0.5% mol, the sheet resistance of each type of film increased.

The films prepared from $Cd_{1-y}Zn_yS$ powder were found to be more resistive than the CdS layers. SEM investigations revealed that $CdCl_2$ was not such an effective flux with the $Cd_{1-y}Zn_yS$ films(Fig 8.4a). In an attempt to develop a flux which would promote the grain growth of the solid solution of $Cd_{1-y}Zn_yS$ varying compositions of $CdCl_2$ + $ZnBr_2$ were explored and good sintering was obtained with a mixture of 15% $CdCl_2$ + 1% $ZnBr_2$ when firing was carried out at 640°C for 60 min in the presence of cadmium vapour. Typical S.E. micrographs of the films prepared with this flux are shown in Fig 8.4b. It is

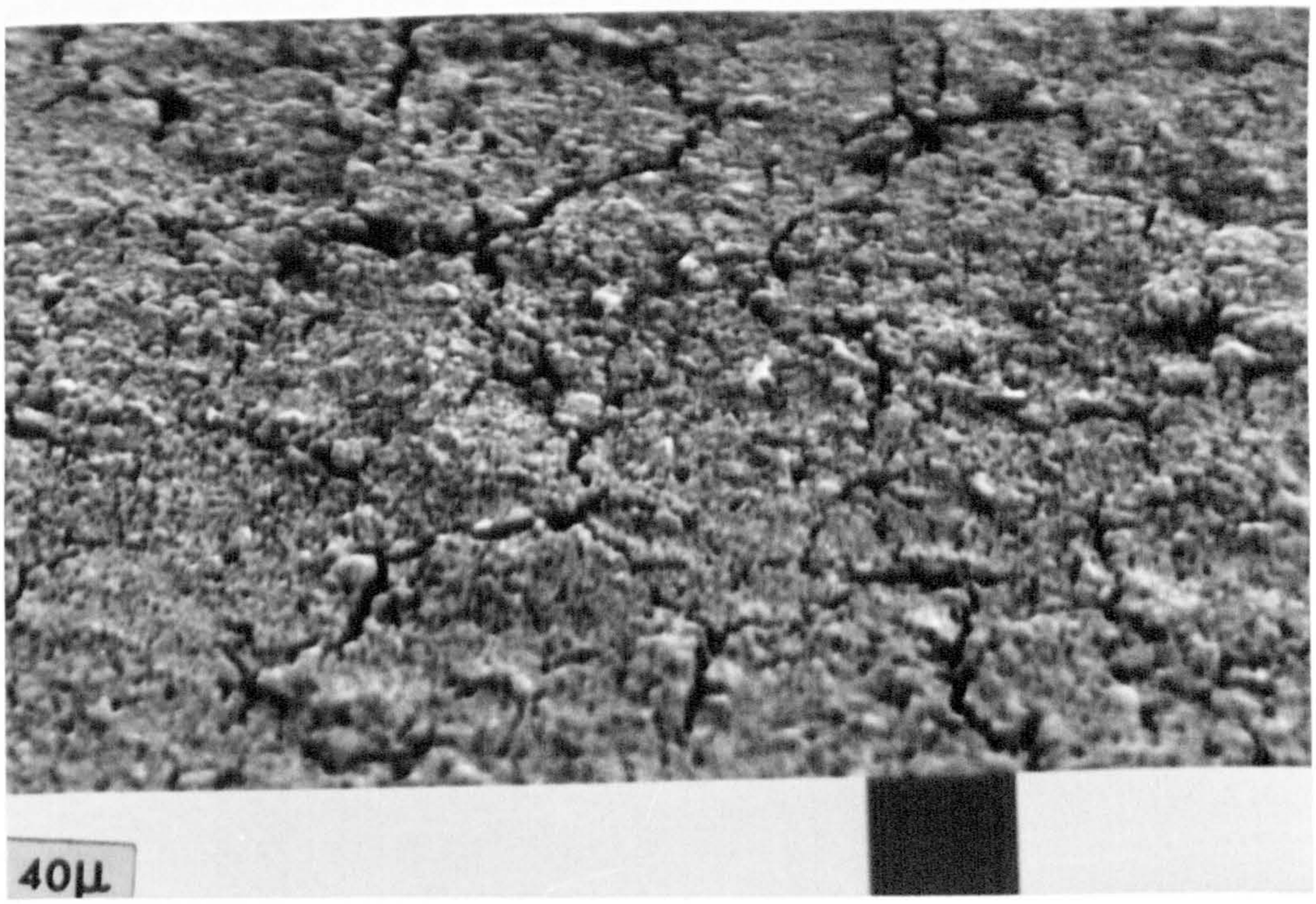


FIGURE 8.4(a): S.E. micrograph of a silk screen sintered $Cd_{0.8}Zn_{0.2}S$ film spread with $CdCl_2$ as flux.

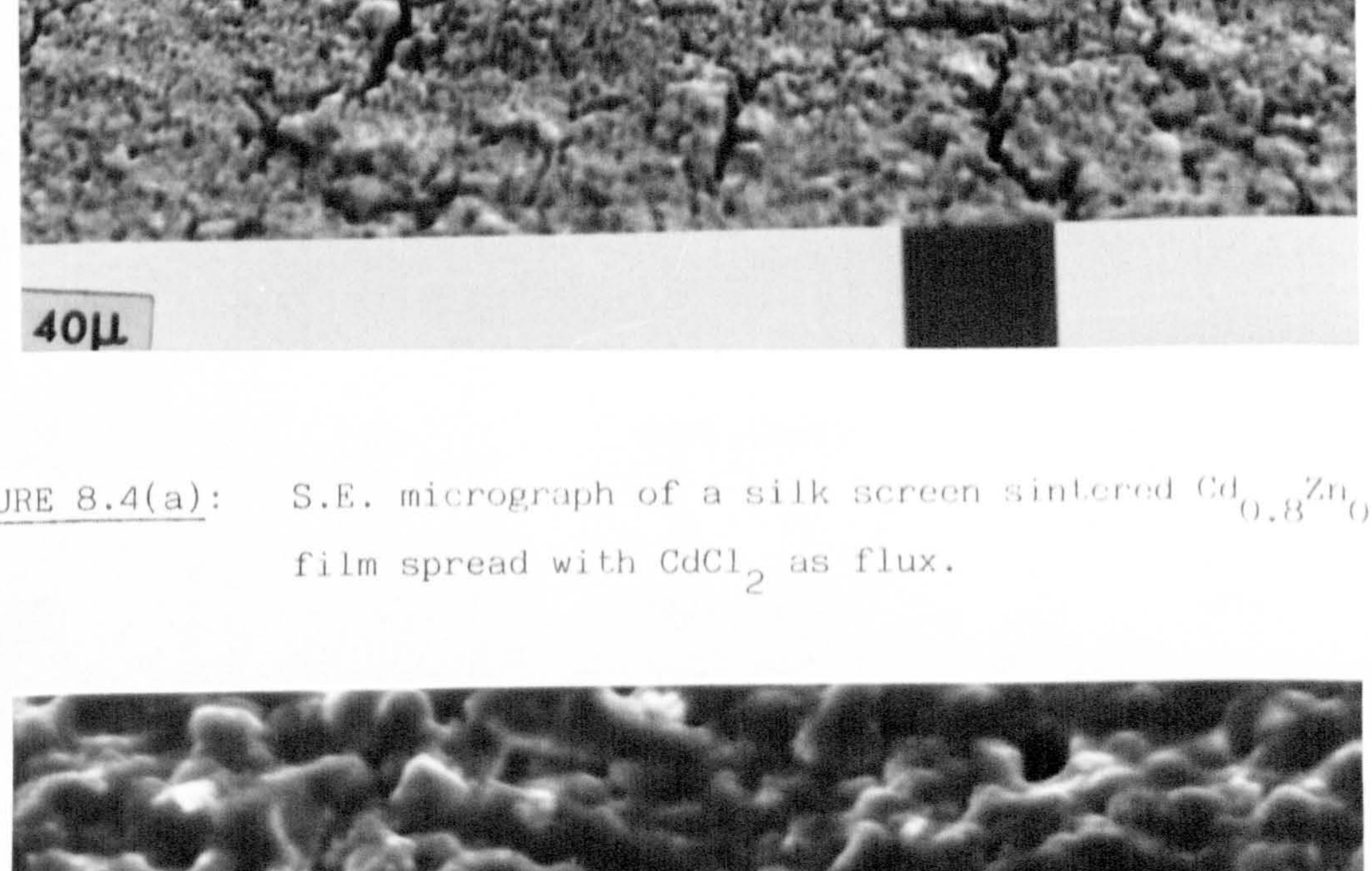


FIGURE 8.4(b): S.E.micrograph of the $Cd_{0.8}Zn_{0.2}S$ film spread with $CdCl_2$(5%) + $ZnBr_2$(1%) as flux.

clear from this figure that the particles of the solid solution of $Cd_{1-y}Zn_yS$ tended to sinter with this particular flux.

The resistance of the layers increased, as expected, with increasing zinc content, and once again indium was included to promote some reasonable conductance. The sheet resistance of the various layers produced are listed in Table 8.2, and it is clear that indium was very effective in lowering the resistance.

TABLE 8.2: Effect of Indium on $Cd_{1-y}Zn_yS$ Films

Composition $Cd_{1-y}Zn_yS$	In Content % mol	Flux used	Sheet Resistance KΩ/□
$Cd_{0.9}Zn_{0.1}S$	-	$CdCl_2$(15%)	3.0
$Cd_{0.9}Zn_{0.1}S$	0.1	$CdCl_2$(15%)	1.8
$Cd_{0.8}Zn_{0.2}S$	-	$CdCl_2$(15%)	40
		$CdCl_2$15%+$ZnBr_2$1%	30
$Cd_{0.8}Zn_{0.2}S$	0.1	$CdCl_2$(15%)	10
		$CdCl_2$15%+ $ZnBr_2$1%	2.2
$Cd_{0.6}Zn_{0.4}S$	0.1	$CdCl_2$(15%)	200
		$CdCl_2$15%+$ZnBr_2$1%	50

The flux also had a remarkable effect on the resistance of the films. With $CdCl_2$ + $ZnBr_2$ as the flux the indium doped sintered films had a resistance four times lower than that of sintered films with $CdCl_2$ as a flux. This may be due to the better sintering of the films of mixed composition reducing the intergranular resistance, which would otherwise dominate and contribute towards the higher resistance.

8.3.2 Heterojunction Properties

After obtaining well sintered and conducting films, heterojunctions (diameter 3 mm) were prepared on a number of samples by the dry barrier process [3,4]. With heterojunctions formed on the films prepared on glass slides, current collection was provided by an indium contact on the CdS near the junction. With films prepared on conducting glass, the tin oxide layer beneath the CdS film provided one of the contacts. Devices were formed on films prepared using different quantities of $CdCl_2$. The device parameters are summarized in Table 8.3 which shows mean values of the performance parameters of five devices formed on each type of film. The parameters presented in the table refer to devices given a 7 min post barrier heat treatment in argon at 200°C.

TABLE 8.3: Device Parameters of Heterojunctions Formed on Films Prepared with Different Quantities of $CdCl_2$.

% of $CdCl_2$ used in making the film	DEVICE PARAMETERS					
	ON FILMS PREPARED ON GLASS SLIDE			ON FILMS PREPARED ON CONDUCTING GLASS SUBSTRATE		
	OCV Volts	SCC mA cm^{-2}	FF	OCV Volts	SCC mA cm^{-2}	FF
8	.52	5	.3	.5	12	.4
10	.51	8	.4	.49	14	.45
15	.51	6	.4	.49	12	.43
20	.46	5	.4	.4	10	.43

It is obvious from this table that the OCV decreased with increase in the quantity of $CdCl_2$. The SCC was highest for the heterojunctions on films prepared with 10% $CdCl_2$. The FFs and SCCs were larger with the devices on conducting glass, although the OCVs were slightly lower. This variation in device performance was probably due to the different arrangements for the current collection. With a view to providing a suitable geometry, particularly with photocapacitance in mind, only devices prepared on conducting glass substrates were used further.

The performance of the devices formed on undoped films and on those doped with a range of indium concentration are compared in Fig 8.5. These reveal that as the indium content was increased, the heating time necessary to optimise the device characteristics increased substantially. While the device made on CdS containing no indium attained its optimum characteristic after 7 min heat treatment in argon at 200^{o}C, the optimum post barrier heating time for the devices formed on films containing 0.001, 0.01, 0.1% mol In was 10, 20 and 30 min respectively. Here 'undoped' implies the films contained no indium. In fact all films were basically doped with fluorine and indium was an additional dopant. In general the OCV and SCC of the devices prepared on indium doped material were always inferior to those of devices prepared on undoped CdS films, but in contrast, the fill factor was invariably much superior when indium doped CdS was used. In the as-prepared condition, the OCV and SCC of devices on the films without indium were 0.4V and 11 mA/cm^2, while those parameters for devices on CdS with the highest indium content (0.1% mol) were 0.1V and 2.5 mA/cm^2. After the heat treatment, the OCV and SCC improved to reach values 0.49V and 14 mA/cm^2 on undoped devices, while values of only 0.38V and 4.5 mA/cm^2 could be obtained with indium doped (0.1% mol) films. The values of these parameters for the devices formed on films doped with 0.001 and 0.01 mol% In were intermediate between the values obtained with devices formed on undoped CdS and CdS with 0.1% mol In. The few attempts which were made to fabricate heterojunctions on indium doped

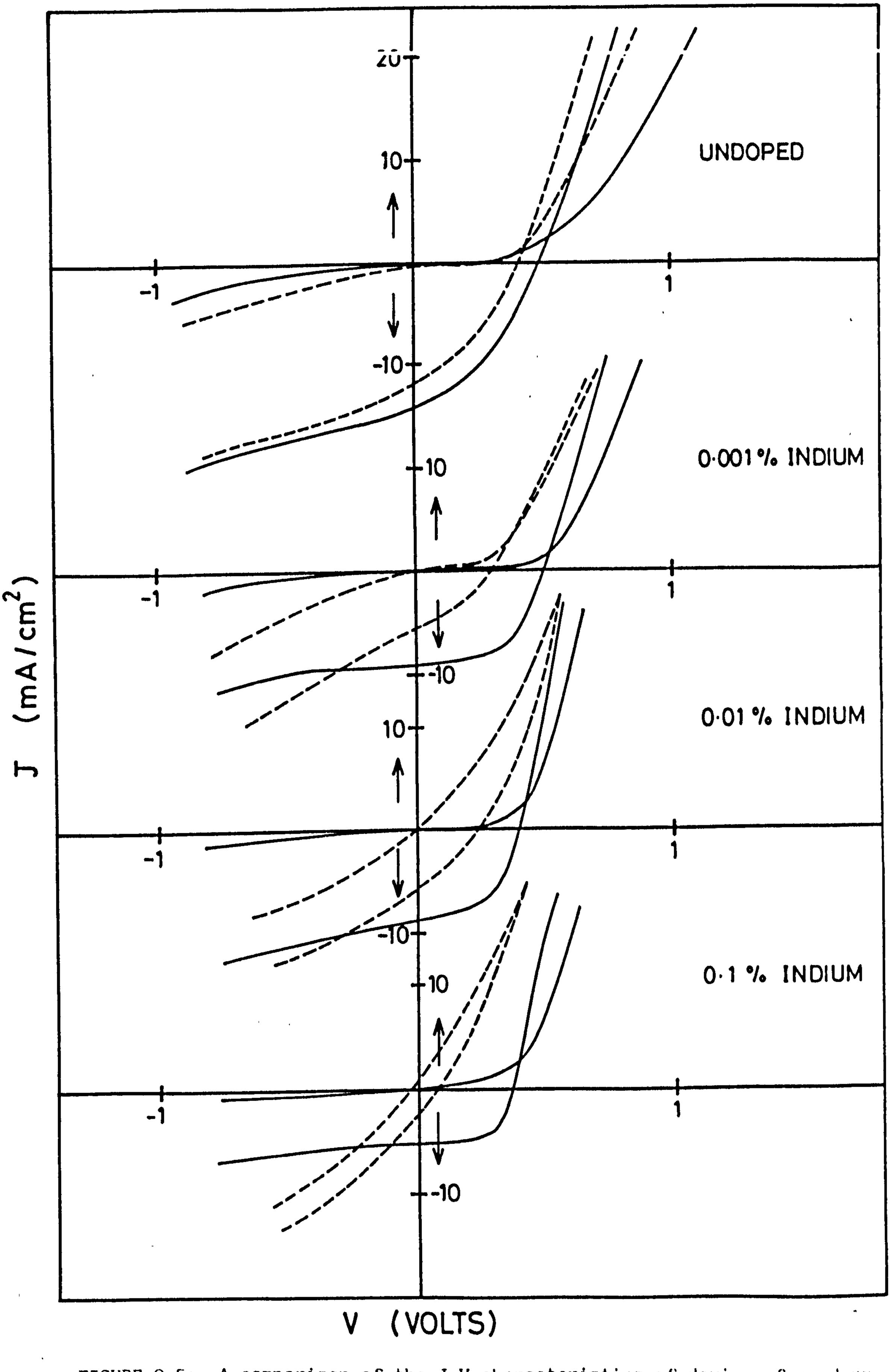


FIGURE 8.5: A comparison of the J-V characteristics of devices formed on films doped with different indium concentrations.

$Cd_{0.8}Zn_{0.2}S$ revealed that the OCV could be increased to 0.55 volts, but the SCC was reduced (4 mA/cm^2).

The spectral responses of devices formed on undoped sintered films, heated for different periods, were recorded at 295K and 85K, but only those measured at the lower temperature are shown in Fig 8.6 because these give a better indication of the phase of the Cu_xS present in the device (see section 5.3.2). With films sintered for a period of 10 min, most of the response occurred at 0.7 μm which corresponds to djurleite[4]. As the sintering time was increased, the response at 0.96 μm increased progressively and was clearly apparent in the response for the devices formed on films sintered for 60 min. During the SEM investigation some regions of dark contrast occasionally appeared (Fig 8.7) and EDAX studies showed that these contained excess chlorine (Fig 8.8). This might be due to inadequate dispersion of $CdCl_2$. When heterojunctions were made on films containing such dark regions, the spectral response was found to contain a broad peak at 0.7 μm indicating the presence of djurleite. The spectral responses at 85K of the devices on indium doped films after heat treatment are shown in Fig 8.9. As the indium content was increased the relative responses at ∿ 0.7 μm progressively decreased while that at 0.96 μm was retained even after the heat treatment.

The spectral responses measured at 295K and 85K for devices heat treated for a long period, shown in Fig 8.10, provide an indication of the effects of doping with indium. The response at 0.96 μm was much larger with the indium doped device whereas the response of the two at about 0.7 μm was comparable at R.T. However at 85K the response at 0.7 μm was enhanced with the undoped CdS.

The photocapacitance spectra of the heat treated devices on indium doped and undoped material were measured both at 295K and 85K and are shown in Fig 8.11. The spectra of the devices formed on the undoped sintered material are similar to those obtained from single crystal CdS devices

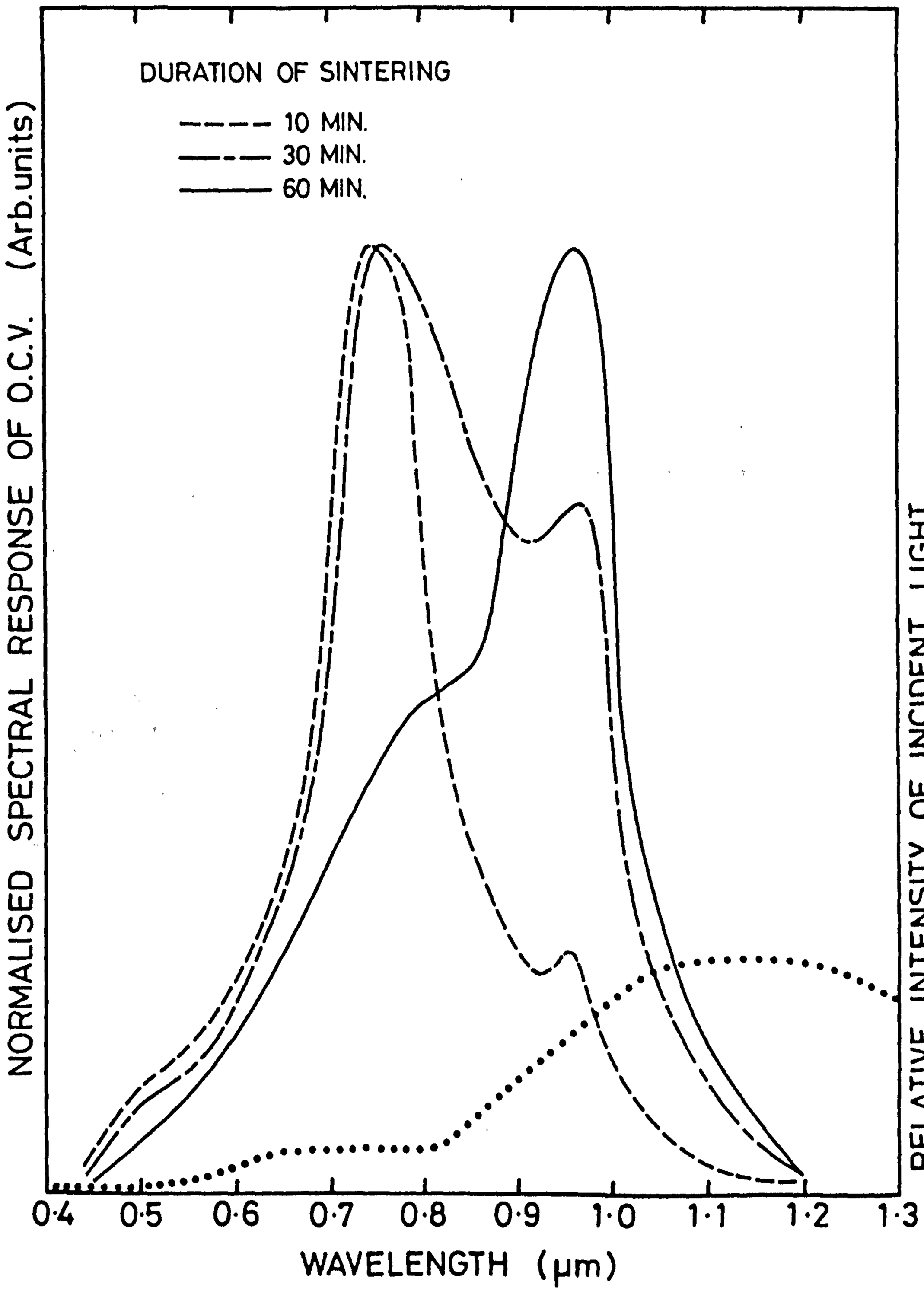


FIGURE 8.6: Spectral response (at 85K) of heterojunctions formed on films sintered for different periods.

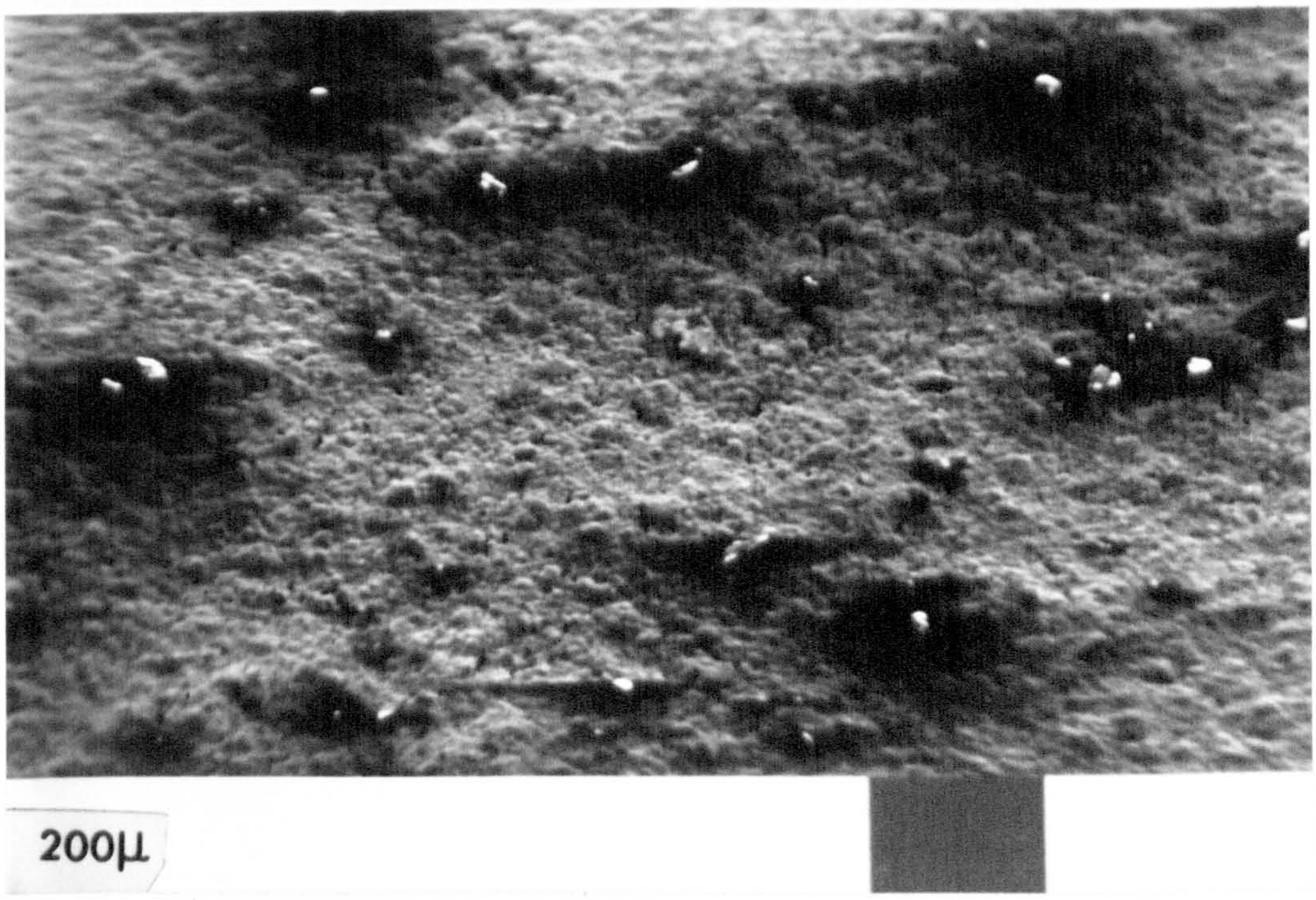


FIGURE 8.7: Dark contrast observed in the S.E.micrograph of a few films

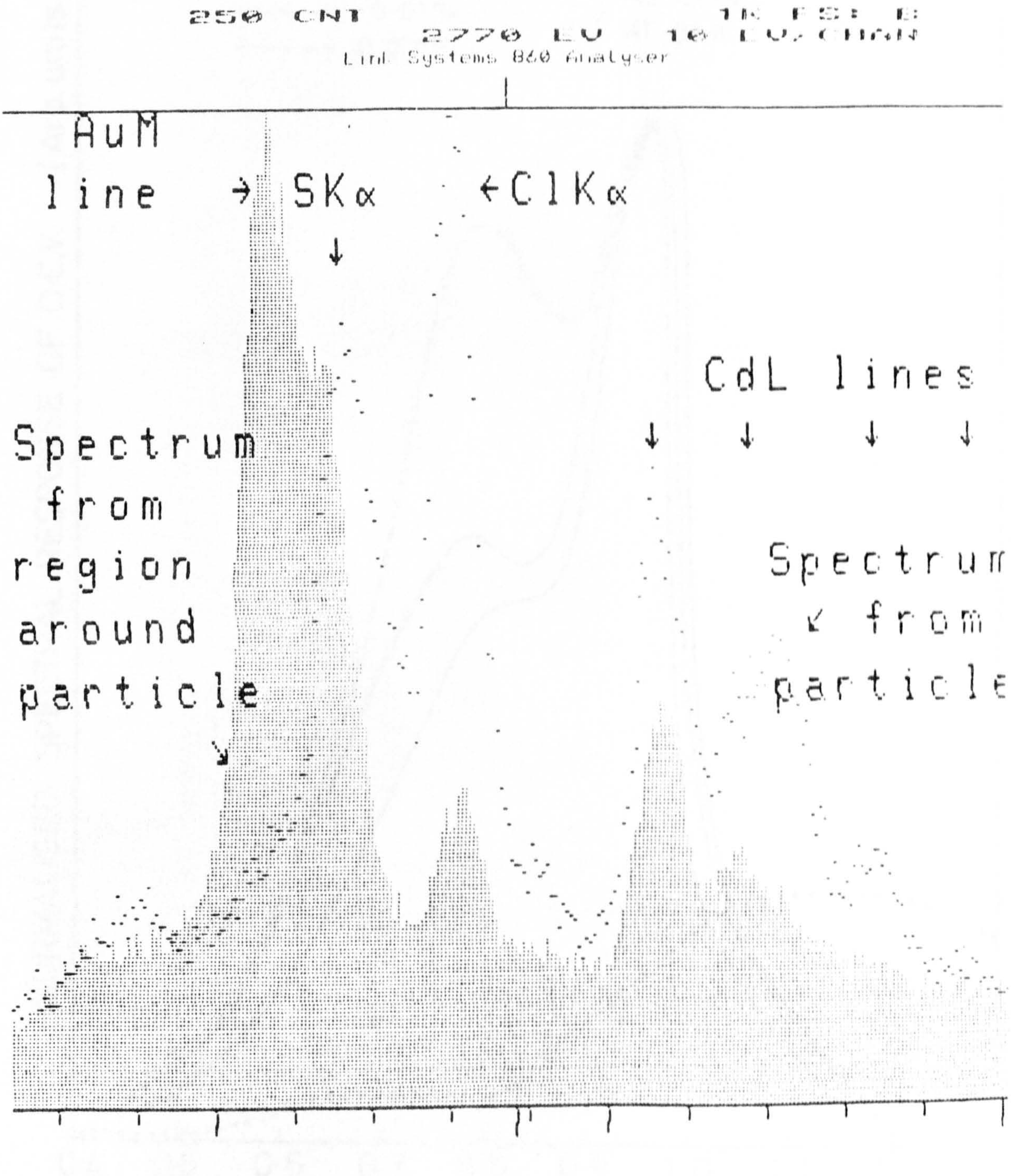


FIGURE 8.8: EDAX spectra for the dark points described in Fig 8.7.

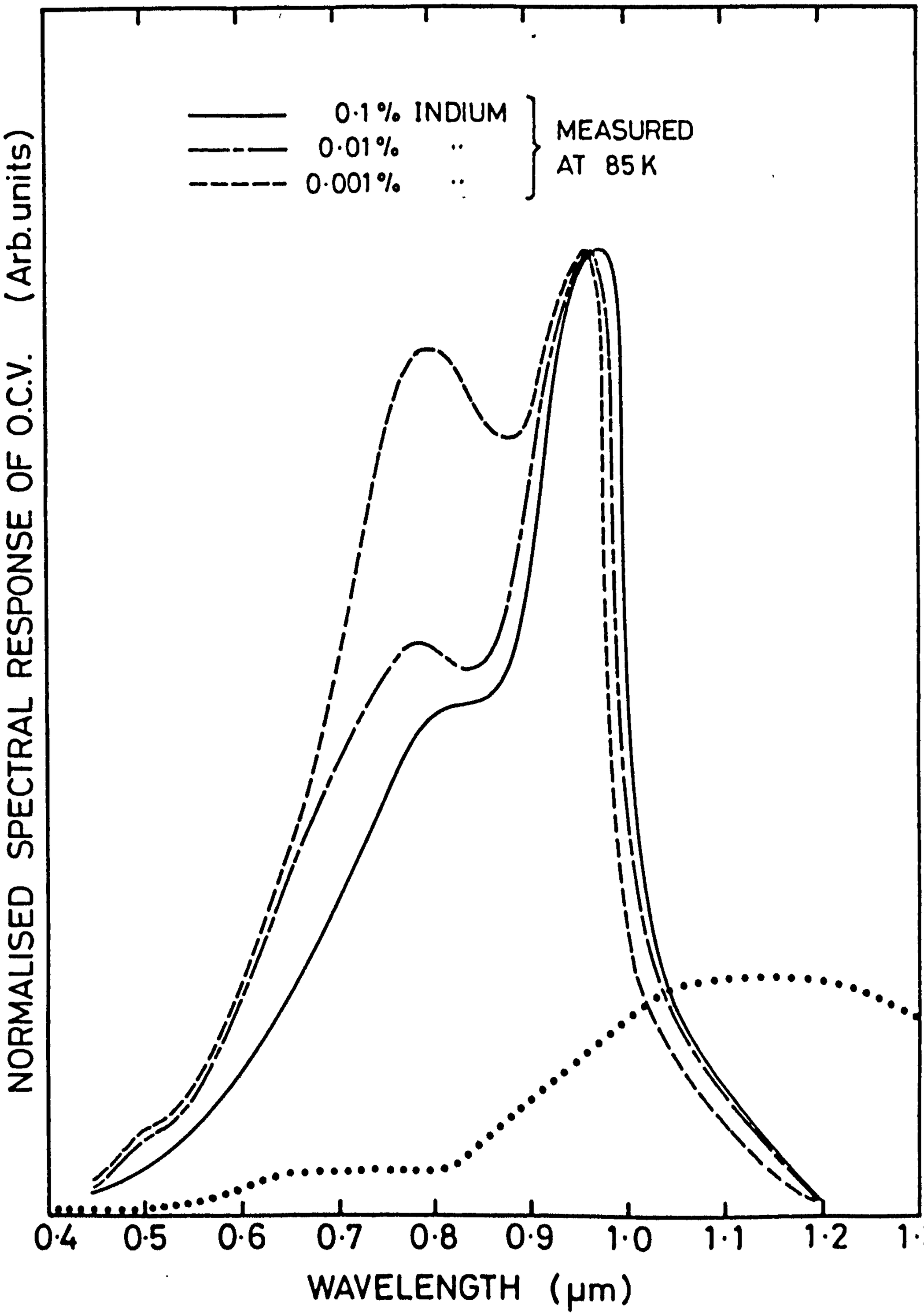


FIGURE 8.9: Spectral response at (85K) of heat treated devices formed on different indium doped CdS films.

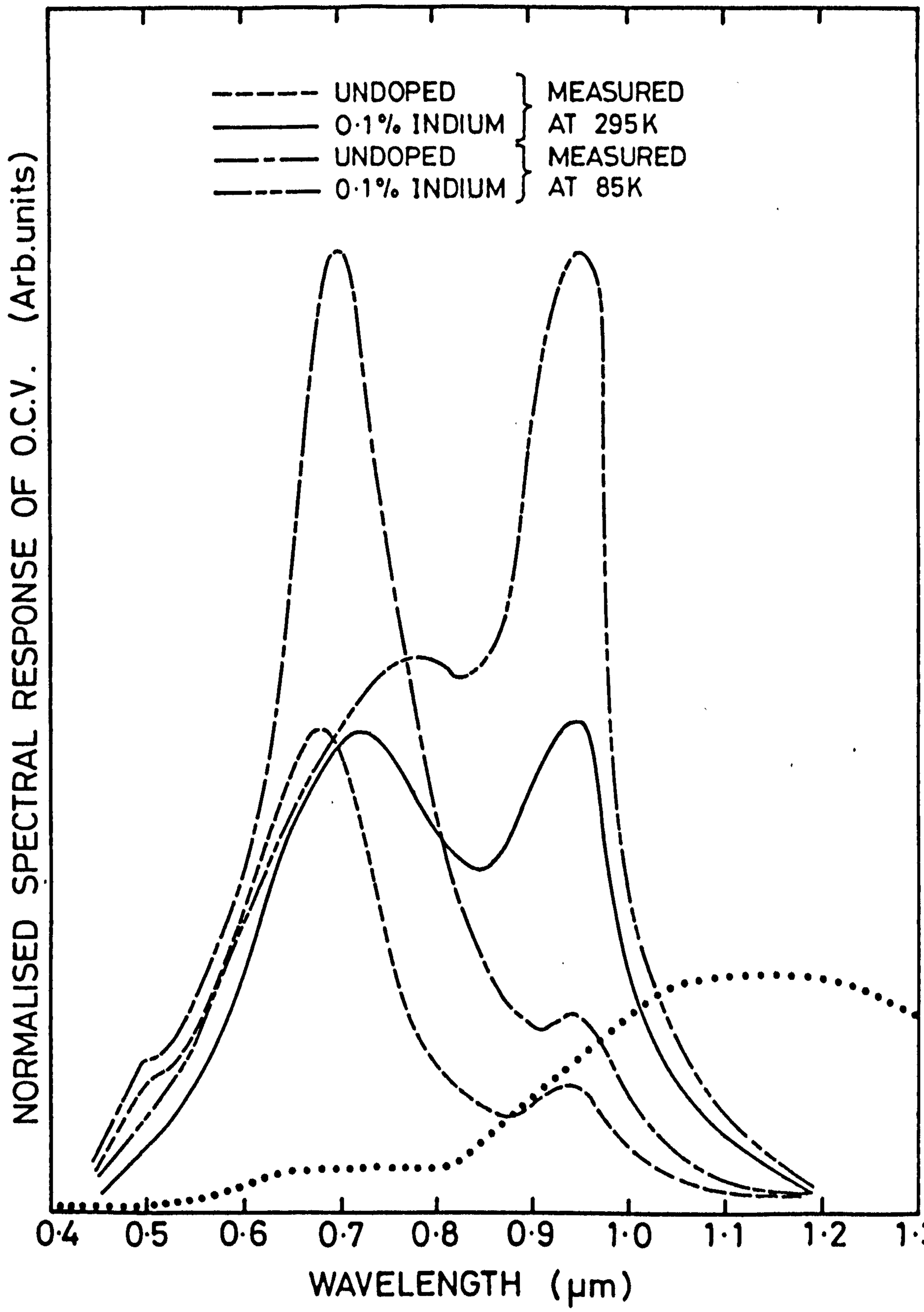


FIGURE 8.10: A comparison of the spectral response of heat treated heterojunctions formed on undoped and indium doped films

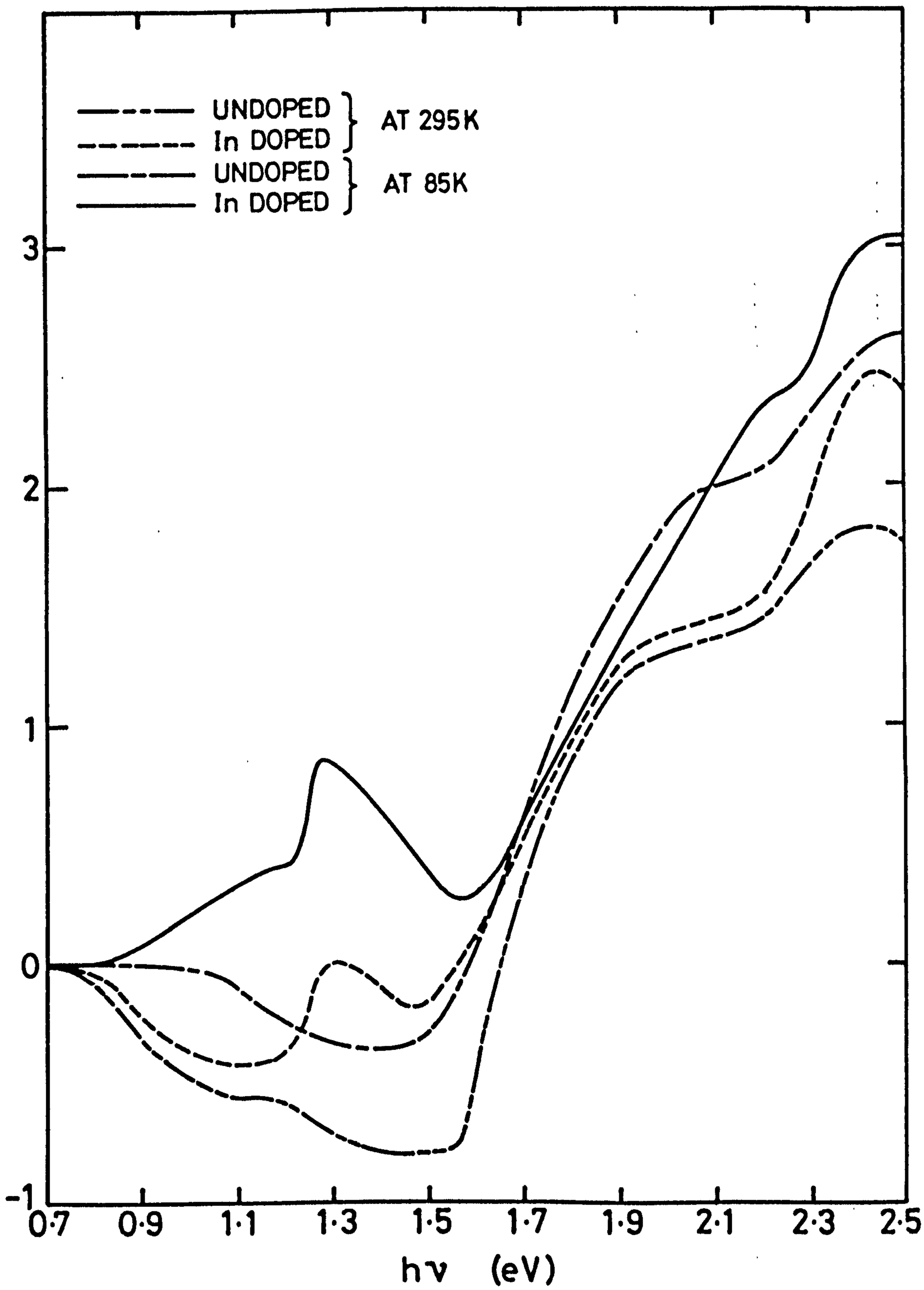


FIGURE 8.11: Photocapacitance spectra of heterojunctions formed on undoped and indium doped films

similarly treated in argon (section 6.4.3). With devices formed on indium doped material, measurements made at room temperature indicated that quenching of the photocapacitance occurred with threshold values of 0.75 and 1.3 eV in addition to the fall in photocapacitance at 2.48 eV. In the same spectrum enhancements of the photocapacitance occurred with onset values of 1.2, 1.5 and 2.2 eV. When measurements of the same indium doped devices were made at 85K, the quenching threshold $\sim$ 0.7 μm was no longer observed but a new enhancement appeared with an onset at 0.8 eV. This enhancement was followed by another positive threshold at 1.22 eV followed by a sharp fall at 1.28 eV. This quenching saturated at 1.55 eV and a further enhancement occurred as with the undoped devices.

8.4 DISCUSSION

In this study of silk screen printed CdS and $Cd_{1-y}Zn_yS$ films for use in the preparation of CdS/Cu_xS and $Cd_{1-y}Zn_yS/Cu_xS$ heterojunctions by the dry barrier process, the first objective was to find the optimum conditions for sintering. A major requirement was to sinter the film at a temperature just below the softening point of the glass substrate. In this connection the use of $CdCl_2$ as a flux in the preparation of CdS films was demonstrated to be particularly effective. This flux has also been used by other workers[1,2,5,6], in preparing silk screen printed films of CdS. It is thought that $CdCl_2$ melts at $\sim$ 568°C and the CdS dissolves in the molten $CdCl_2$. The sintering process promotes particle fusion and granular regrowth at a relatively low temperature[7]. However, with the $Cd_{1-y}Zn_yS$ films, $CdCl_2$ was not so effective. This is due to the zinc content which probably inhibits the process of the dissolving of solid solution in $CdCl_2$. However a flux comprising 15% $CdCl_2$ and 1% $ZnBr_2$ was investigated and seemed to work better than $CdCl_2$ with the $Cd_{1-y}Zn_yS$ films.

The amount of $CdCl_2$ needed to provide good sintering depends on the particle size. For the films prepared from powder which had been swing

milled for 2 min, 10% was adequate, while the films from powders swing milled for 15 min, 20% $CdCl_2$ was required. With the increase in the swing milling time, the particle size decreases and the surface area increases. This means that the same amount of $CdCl_2$ has to be spread over a larger surface area and therefore would be less effective. However, there is no linearity between the probable increase in the surface area and the quantity of $CdCl_2$ required. Perhaps the surface area of the smaller particles is modified by the formation of clusters. The higher sheet resistances of the films containing the smaller particles indicate the reducing effect of the flux.

Some of the $CdCl_2$ re-evaporates when the films are fired at 610°C for long periods (∿ 1 hr). However remnants of chlorine may remain in the film if the sintering time is short, and this might affect the device performance adversely[8]. The spectral response measurements of the devices formed on films sintered for different periods (see Fig 8.6) show that extending the sintering time gave rise to a predominant response at 0.96 μm which corresponds to the chalcocite phase of Cu_xS. On the other hand, the devices formed on films sintered for a shorter period had their main response at ∿ 0.7 μm, indicating the presence of the djurleite (Fig 8.6). This may be attributed to excess chlorine which Palz et al[8] have suggested affects the phase of Cu_xS. The presence of chlorine has also been found to have a deleterious effect in CdS/CdTe silk screen printed heterojunctions[9], where this has been attributed to the donors created in the p-type semiconductor by chlorine. It has been shown in the present work that devices formed on sintered surfaces on which particles of $CdCl_2$ are still present have a predominant djurleite response. It appears therefore that the formation of efficient CdS-Cu_2S heterojunctions requires the removal of any excess of $CdCl_2$ before the barrier is formed.

The effect of excess $CdCl_2$ on the device characteristics was also readily apparent (Table 8.1). The poor SCC of the devices formed on films prepared

with more than 10% of $CdCl_2$ could be attributed to the formation of the undesirable phase of Cu_xS[10] while the reduction in OCV may be due to the increased number of donors[11]. The J-V characteristics (Fig 8.5) show poor fill factors, even with the better devices, which can be attributed to the high series resistance. The purpose of introducing indium into these films was to reduce their resistivities. Indium is known to provide donors in CdS and has been used extensively to obtain conducting films[12-16]. In fact, one of the initial reasons for using indium was to reduce the sheet resistance until it became comparable with that of the conducting glass. This would have made the conducting glass redundant and simultaneously avoided the probability of short circuiting which can occur in films deposited in conducting glass due to pin holes or other shunting paths. The use of indium was quite effective in reducing the resistivity of both CdS and $Cd_{1-y}Zn_yS$ films (Tables 8.1, 8.2). However, increasing the indium content beyond 0.1% mol led to an increasing resistivity. This is probably a grain boundary effect[17,18]. Unfortunately the device characteristics were rather poor, and the low OCV might be attributed to the lowering of the potential barrier with increased donor content[14,19]. In their as-prepared condition, the indium doped CdS layers remain uncompensated and very long heat treatments are required to compensate these donors with diffusing copper. The improved fill factors demonstrate the low series resistance of the devices.

An important point is that the SCC from devices on indium doped material was rather low in spite of the excellent spectral response of the long heat treated devices with a predominant peak at 0.96 μm. The photocapacitance studies revealed an additional feature with indium doped material. The spectrum shown in Fig 8.11 can be understood in terms of four levels in the depletion region (Fig 8.12). The quenching of the photocapacitance at R.T. at 0.75 eV in devices on In doped material also show that copper does diffuse in CdS. However, since this quenching at 0.7 eV disappears at L.N. temperature and an enhancement at 0.81 eV is observed in devices on indium

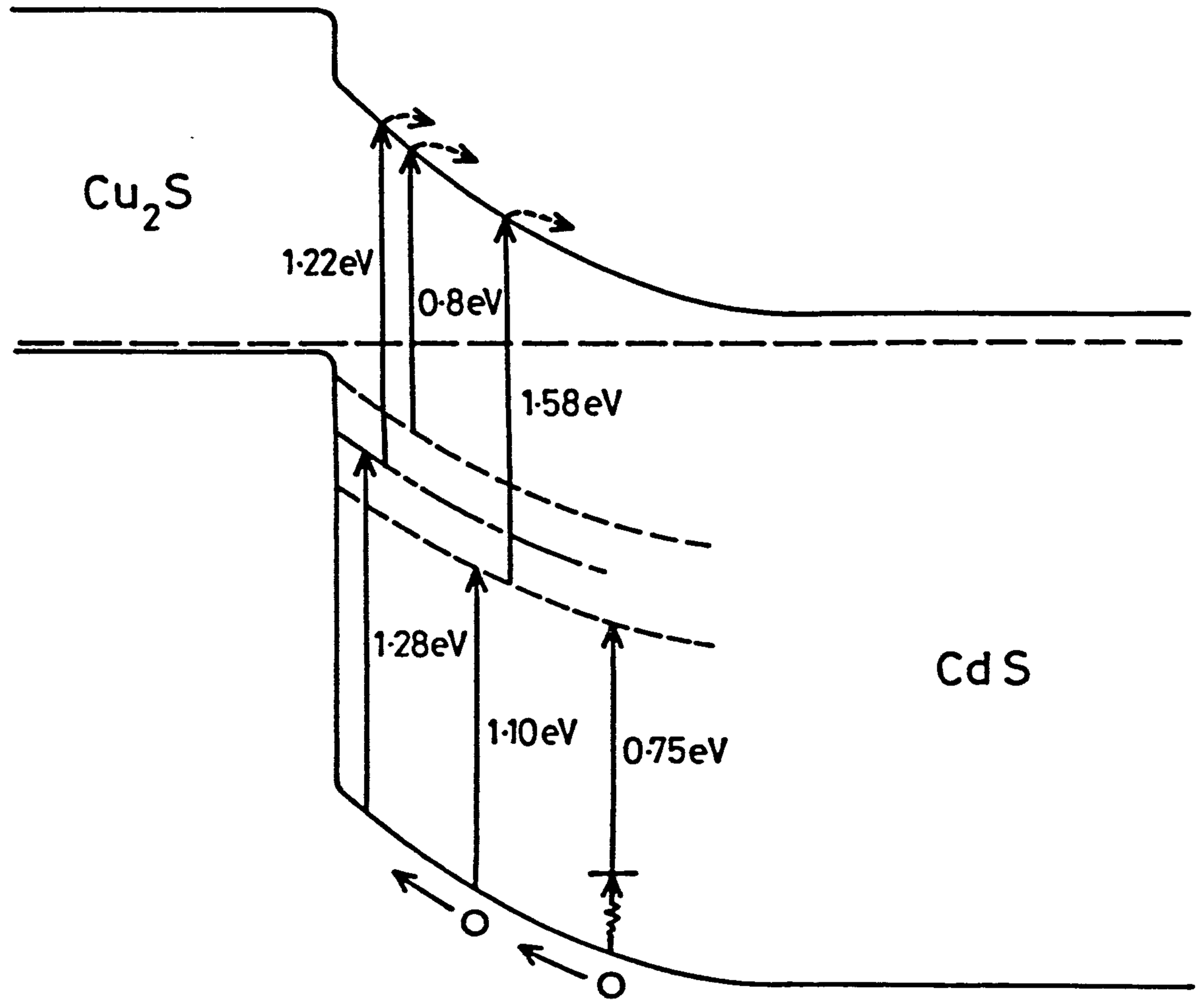


FIGURE 8.12: Energy band diagram showing quenching and enhancement processes of photocapacitance in the heterojunctions formed on indium doped films

doped material, it seems that the dominating process is now an excitation of electrons from a donor level situated at 0.81 eV below the conduction band. Such a level in CdS has been found by Nicholas and Woods[20] and also reported by Rothwarf[21]. Our observations suggest that the formation of such a trap is augmented by the incorporation of indium in CdS. An additional feature in the spectrum is the increase in photocapacitance at 1.22 eV which may be due to the excitation of electrons from a recombination centre located 1.28 eV above the valence band. The fall in photocapacitance with an incident photon energy of 1.28 eV reveals the same trap but now the dominating process is the excitation of electrons from valence band to this level. This centre which is observed only in the photocapacitance spectra of the devices on indium doped material might be associated with a complex of In and cadmium vacancies which is supposed to form a very mobile pair[22].

The red response of heat treated devices on indium doped CdS is probably due to this centre. Similar effects of enhanced red response have been observed in CdS containing excess Cd where a deep centre 1.2 eV below the conduction band was reported[23]. Our results have also shown that the SCC deteriorates when indium is incorporated. It is reasonable to suggest therefore that the recombination centre located at 1.28 eV above the valence band affects the SCC of devices on indium doped CdS.

The attempts made here to prepare silk screen printed films of indium doped $Cd_{1-y}Zn_yS$ have not led to more efficient devices. Although the lattice mismatch is minimised and the barrier height is increased[24,25], with the inclusion of zinc, the resistivity of the films increased. Again the resistivity can be lowered by incorporating indium, but the barrier height is then reduced and J_o increases, reducing the OCV. With a few devices formed on a film of $Cd_{0.8}Zn_{0.2}S$ with 0.1% In, the OCV was found to be as high as 0.55V. However, the SCC was a rather poor 4 mA/cm^2.

8.5 CONCLUSION

It has been shown that the process of silk screen printing can be used to obtain films of CdS and $Cd_{1-y}Zn_yS$ suitable for use in fabricating heterojunctions. Smooth films of CdS were prepared using a thixotropic slurry obtained by mixing CdS powder swing milled for 2 min in $\sim$ 28% of propylene glycol (binder) and 10% of $CdCl_2$ (flux). On sintering at 640°C for 60 min in argon in the presence of cadmium vapour, films were obtained with surfaces with the appearance of partial melting. Successful hetero-junctions were made on such films. With $Cd_{1-y}Zn_yS$ films, a mixture of $CdCl_2$(15%) + $ZnBr_2$(1%) proved to be a better flux. The effect on the resistivity of introducing indium was quite obvious but unfortunately the junction parameters were inferior. The cause of the reduced current density on the highly conducting films was probably due to a recombination centre 1.28 eV above the valence band. A similar centre was observed in the devices on $Cd_{1-y}Zn_yS$ single crystal substrates (section 6.4.3). It was also demonstrated that the presence of excess $CdCl_2$ adversely affected the phase of Cu_xS.

REFERENCES TO CHAPTER 8

1. H. Matsumoto, N. Nakayama and S. Ikegami, Jap.J.App.Phys. 19 (1980) p.129

2. D.P. Amalnerkar, M.S.Setty, N.R.Pavaskar and A.P.B.Sinha, Bull.Matter.Sci.2 (1980), p.251.

3. T.S.TeVelde, Energy Conversion 15 (1975) p.111.

4. P.C.Pande, G.J.Russell and J.Woods, Proc.5th E.C. Photovoltaic Solar Energy Conf. Athens, Greece (1983), p.171.

5. S. Vojdani, A.Sharifnai and M.Doroudian, Electronics Letts. 9 (1973) p.128.

6. F.J.Garcia and M.S.Tomar, Jap.J.Appl.Phys. 22 (1983) p.535.

7. A.G.Stanley, Applied Solid State Science, Advances in Materials and Device Research, Vol.5 (1975). p.251.

8. W. Palz,J.Besson ,T.N.Duy and J.Vedel,9th IEEE PVS Conf.Silver Springs, New York, 1972, p.91.

9. H. Matsumoto, A. Nakano, H. Uda, S. Ikegami and T.Miyazava, Jap.J. App.Phys. 21, (1982), p.800.

10. A. Rothwarf and H.Windawi, Proc.14th IEEE Photovoltaic Specialists Conf. San Diego, California,(Jan. 1980), p.722.

11. R.V.Kantariya, S.Y.Pavelets, T.M.Razykov, G.Y.Umarov and G.A.Fedorus, Sov.Phys.Semicond. 12 (1978), p.960.

12. T.H.Weng, J.Electrochem.Soc. 126 (1979), p.1822.

13. R.H.Bube, F.Buch, A.L.Fahrenbruch,Y. Y Ma and K.W.Mitchell, IEEE Trans Electron Devices. ED-24 (1977) p.487.

14. M. Uekita, K.F.Nelson, C.W.Bates Jr, J.B.Mooney and J.M.Recktenwald, Thin Solid Films, 88, (1982), p.275.

15. J.C.Joshi, B.K.Sachar and P.Kumar, Thin Solid Films, 28 (1982)p.189.

16. F.Z.Nataren, B.Bouchikhi, S.Chandrasekhar,J.P.Crest and S.Martinuzzi, J.Crystal Growth 59 (1982), p.409.

17. L.D.Partain, G.J.Sullivan and C E.Birchenell, J.Appl.Phys. 50 (1979), p.551.

18. D.Eger, A.Zemel H.Shtrikmen and N.Taw ri, Matter.Res.Bull.15 (1980), p.1333.

19. S. Banerjee and H.Saha, J.Phys.D Appl.Phys. 16 (1983) p.185.

20. K.H.Nicholas and J.Woods, Brit.J.Appl.Phys. 15 (1964), p.783.

21. A.Rothwarf, Solar Cells 2 (1980), p.115.

22. E.D.Jones and H.Mykura, J.Phys.Chem.Solids 39 (1978), p.11.

23. A.E.Spakowski, A.E.Potter and R.L.Schalla, Proc.Photovoltaic Specialists Conf.5th, PIC;Sol.209 , (1966),Sect.6-7 .

24. W.Palz, J.Besson, T.Nguyen Duy, J.Vedel, Proc.10th.P.V.S.C. Palo Alto (1973), p.69.

25. L.C.Burton, Solar Cells.1 (1979/80), p.159.

CHAPTER 9

THERMALLY EVAPORATED FILMS OF CdS AND CdS-Cu_2S HETEROJUNCTIONS

9.1 INTRODUCTION

There is a continued interest in CdS-Cu_2S cells formed on evaporated films of CdS as evidenced by the recent developments in Germany where the Nukem Company is going into production in collaboration with the department of Physical Electronics in the University of Stuttgart[1]. For completeness it was decided to extend the study of the dry barrier process to this form of CdS. Various batches of films were deposited by varying the substrate temperature and the evaporation rate. The electrical and structural properties of these films were then characterised and the properties of the heterojunctions and Schottky devices produced on them were studied. Measurements of the current-voltage characteristics, spectral response and photocapacitance were carried out to identify the parameters which were responsible for any changes in the behaviour of the devices. The understanding developed during the course of this work on different forms of CdS was then utilised to explain the results obtained with these films.

9.2 PREPARATION OF FILMS

The schematic diagram of the vacuum system used for producing the films is shown in Fig 9.1. The system was built by Edwards High Vacuum Ltd around a 18" oil diffusion pump to maintain a pressure of about 10^{-5} Torr during the evaporation cycle. The bell jar fixtures are shown in Fig 9.2. The substrates were heated indirectly by an infrared lamp ($_{1000W}$). The temperature of the substrate was controlled by a Eurotherm controller using a NiCr/NiAl thermocouple which was clamped at the top of the substrate. A second thermocouple was used to measure the substrate temperature separately during the evaporation cycle. The deposition rate was determined with the help of a

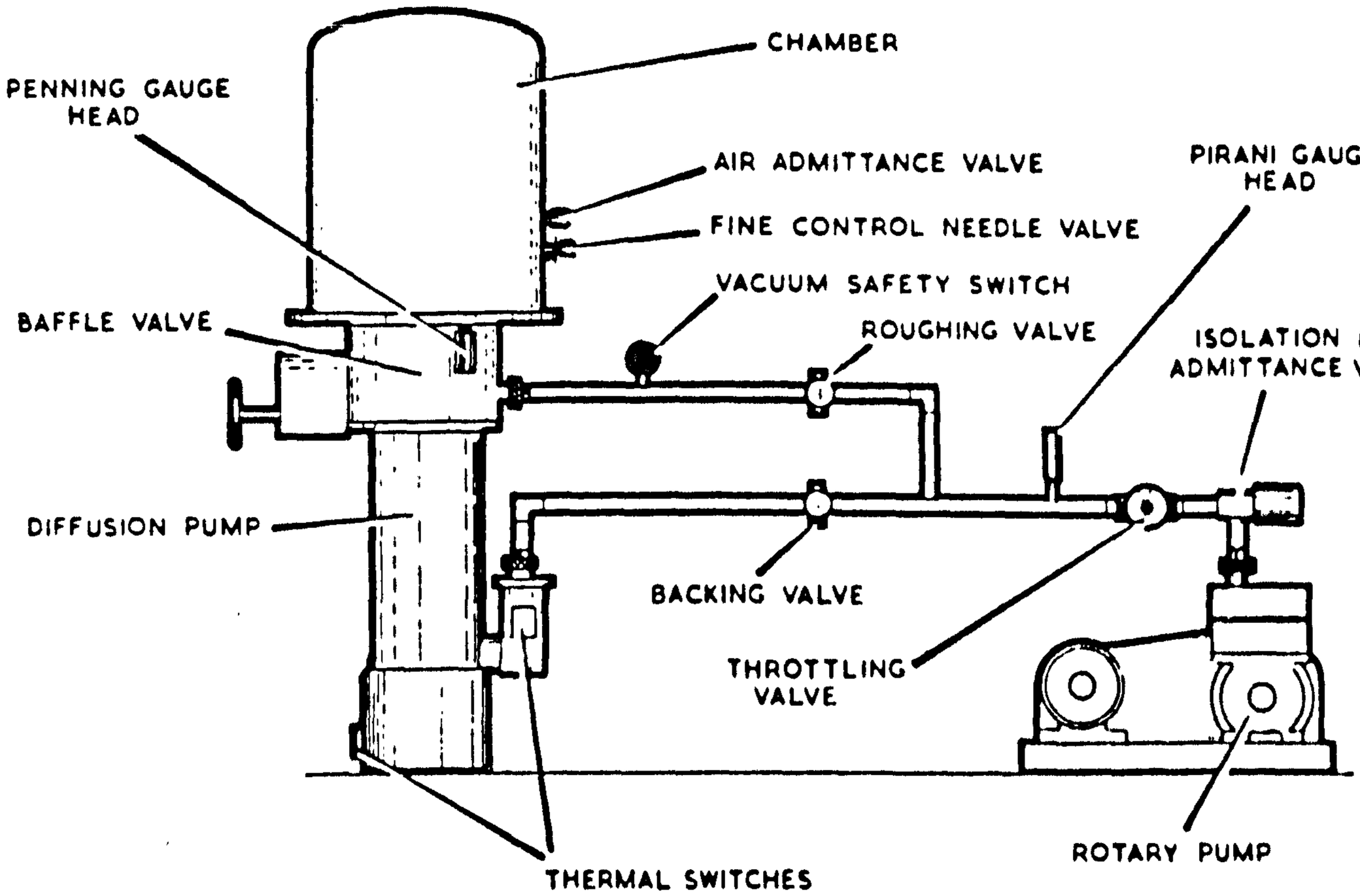


FIGURE 9.1: Schematic diagram of an 18" evaporator

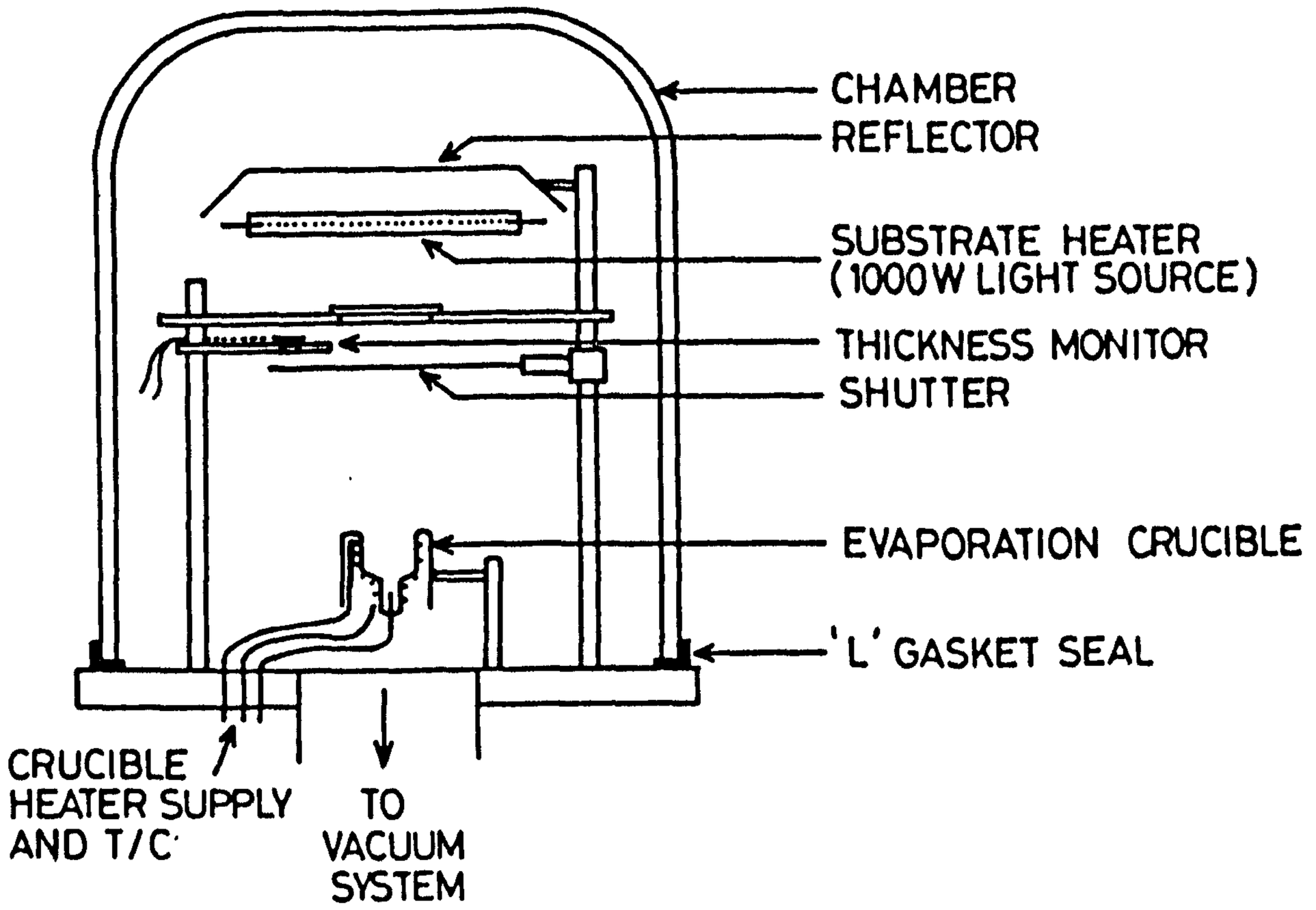
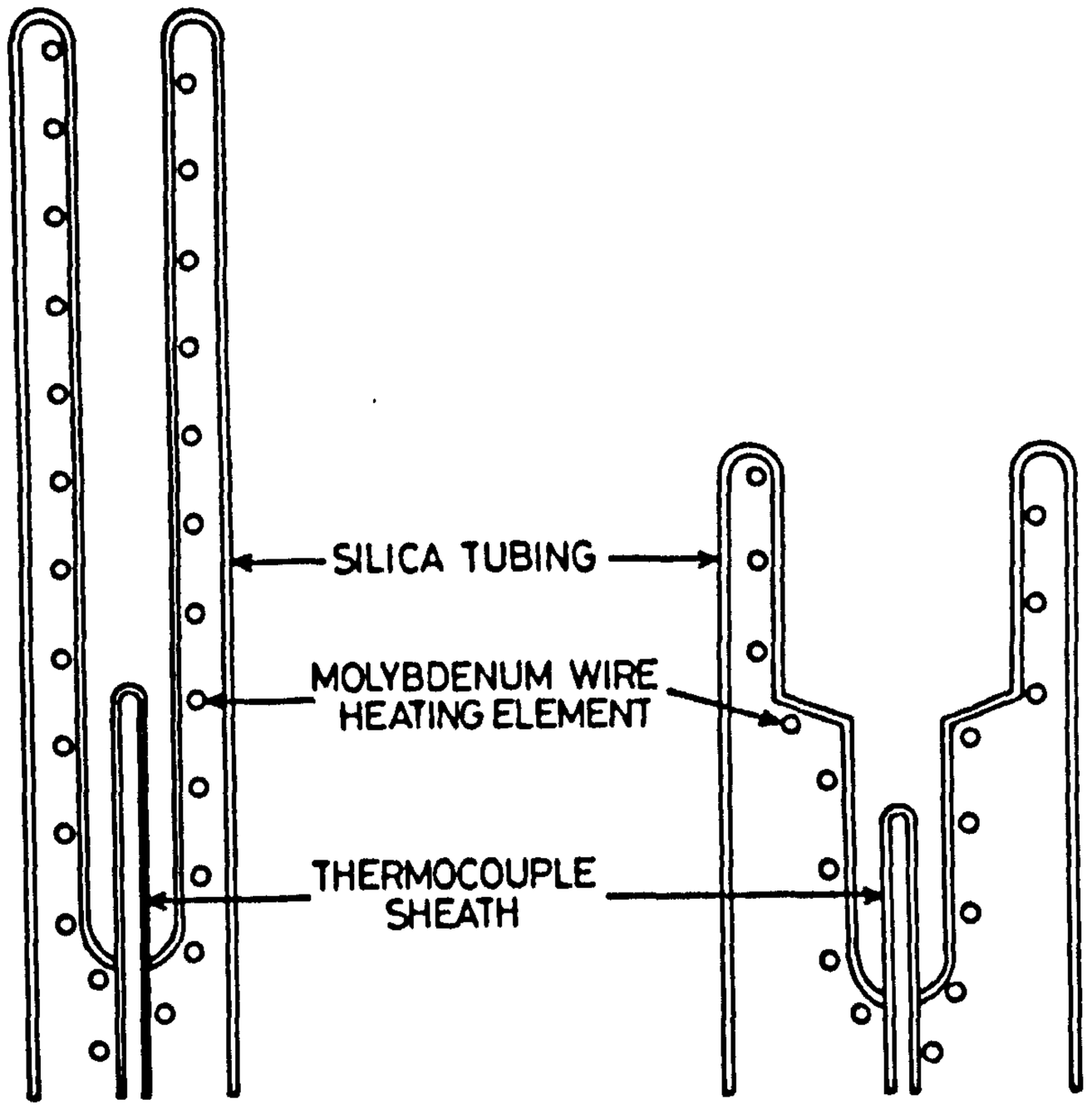


FIGURE 9.2: Bell Jar fixtures for the evaporator used in the deposition of CdS.

quartz crystal thickness monitor. It was found that for the range of thicknesses required (10-20 μm) continuous exposure of the quartz crystal overloaded it, and an arrangement was made therefore to minimize the deposition of CdS on the crystal during the time when the rate was not measured. The crystal holder was fixed on to the same rod which operated the shutter through a rotary seal. This allowed the crystal to be moved away from the substrate after measuring the evaporation rate. At the same time the mechanical shutter could be positioned above the crucible so that the source could be outgassed before deposition on to the substrate began.

Several types of silica crucible were used. Two of them are shown in Figs 9.3a and 9.3b. The crucibles were wound spirally with molybdenum wire. The enclosure of the filament coil between the two walls of the crucible minimized the probability of contamination of the evaporated CdS by the heated filament. The Knudsen crucible shown in Fig 9.3a provided a much more collimated beam and produced a patch on the substrate at about 16 cm above the crucible. In view of this the crucible shown in Fig 9.3b was used, where the length was reduced and a wider opening at the top was provided. This crucible was found to provide a uniform deposit on to five substrates some 20 cm above it. However the maximum rate of evaporation which could be achieved with this source was only 0.65 μm/min. In order to increase the evaporation rate further, a directly heated tantalum crucible was used. The schematic diagram of this crucible is shown in Fig 9.3c. An evaporation rate as high as 1.25 μm/min could be obtained with this source. The source temperature was measured using a Pt(13 %) Rh/Pt thermocouple. With the silica crucible, the thermocouple junction touched the bottom of the crucible nearest the charge via a special narrow tube provided for this purpose (Fig 9.3a). With the tantalum crucible the thermocouple was provided with a thin silica sleeve and inserted in the charge from the top of the crucible.

Commercially produced CdS (B.D.H. optran grade polycrystalline lump) was purified by sublimation in the so-called flow run process. For this,



Silica Crucibles

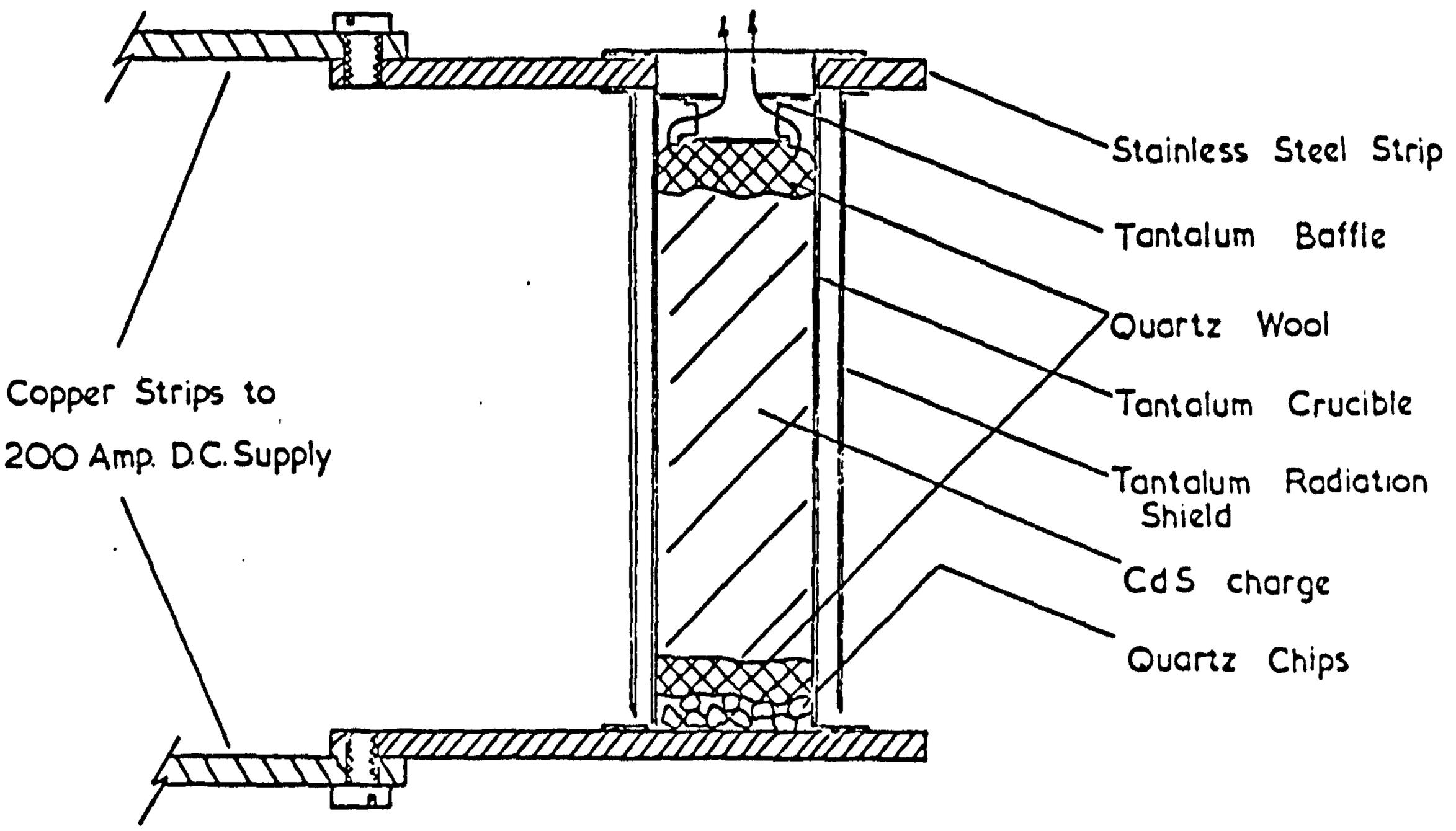


FIGURE 9.3: Evaporation sources used in this study.

the charge was heated to 1150^{o}C in a long silica tube, and a stream of 0.2 l min^{-1} of argon was passed over it. Rods and platelets of yellow crystalline CdS were deposited down stream in a cooler part of the tube. In this process the volatile impurities are carried away to exhaust, while less volatile impurities such as Zn, Fe or Mn are left in the residue of the charge. The sublimed CdS produced in this way was lightly crushed and this provided the source material for all the evaporated layers produced.

The substrates used were either commercially available tin oxide coated glass, or glass slides coated with silver and chromium. The latter ones were fabricated by us. For this, ordinary glass slides were cleaned thoroughly as discussed previously (section 8.2,2). Electron beam evaporation was used to put down successive layers of chromium and silver on the glass substrate. In the electron beam evaporator (Fig 9.4) the hot molybdenum filament was optically screened from both the source and substrate by the negatively biased focussing cage and washer. The electrons were focussed on to the surface of the evaporant which was contained in one of the four graphite crucibles in the water cooled hearth. Two separate crucibles were loaded with chromium and silver respectively. Each crucible could be positioned below the emitter by a lateral movement of a bellow seal. A 10 kV variable power supply was used to provide the accelerating potential. A stabilized beam power of 150 mA, 10 kV could be obtained.

A thin layer (500 Å) of chromium was first deposited at a rate of 50 Å/min on to the cleaned glass slides held at 300^{o}C. The crucible containing silver was then positioned, and a layer of silver about 1 μm thick was deposited on to the chromium. The advantage of the procedure is that chromium adheres very well to glass and silver sticks well to chromium. CdS forms good films on Ag/Cr, whereas it tends to peel off tin oxide coated glass.

The crucible was usually filled with 12 gm of CdS for each evaporation. A thin layer of quartz wool baffle was provided at the mouth of the crucible

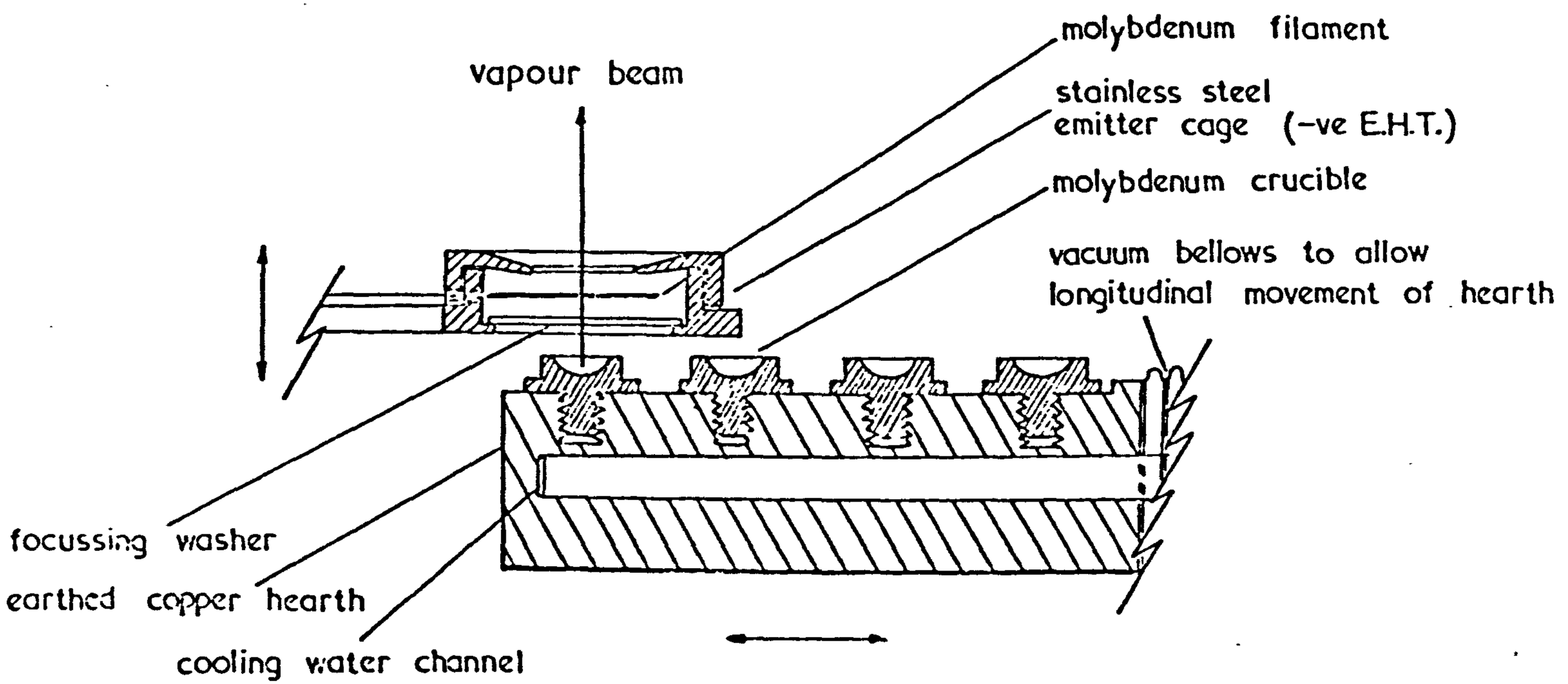


FIGURE 9.4: Genevac Electron Beam Evaporator, type EBU1

to prevent spattering. The evaporation cycle proceeded as follows:

(i) The system was evacuated to 10^{-5} torr, and the substrate was heated to the desired temperature (150-240^{o}C) for ½ hr.

(ii) The filament current was increased gradually until the charge reached 550^{o}C. The CdS powder was outgassed for 30 min at this temperature and then the temperature was increased to between 700 and 1100^{o}C. Once steady state conditions were reached, the mechanical shutter was opened and the evaporation rate was measured. The temperature of the substrate was found to increase by 20-30^{o}C during the evaporation. A typical graph of the variation of substrate temperature during the evaporation and cooling cycles is shown in Fig 9.5. For convenience the substrate temperature reported in this study is the temperature set by the Eurotherm temperature controller.

(iii) At the end of the operation (25-30 min), the mechanical shutter was closed and the source and substrate heating were switched off.

(iv) The substrate was allowed to cool to room temperature and then removed from the vacuum system.

The films produced were then characterized. Their electrical and structural properties were measured and finally heterojunctions were made on each film using the dry barrier process.

9.3 STRUCTURE OF THE FILMS

The structure of the films was investigated by RHEED and their cross-section was examined in the SEM. The RHEED patterns corresponding to three films deposited at substrate temperature (T_S), 150, 200 and 240^{o} C are shown in Fig 9.6. A better defined (spottier) RHEED pattern was obtained as the substrate temperature was increased which indicates an improvement in the crystalline order in the films grown at 200^{o}C. However at higher substrate temperatures still the arcs again appeared. For layers deposited at

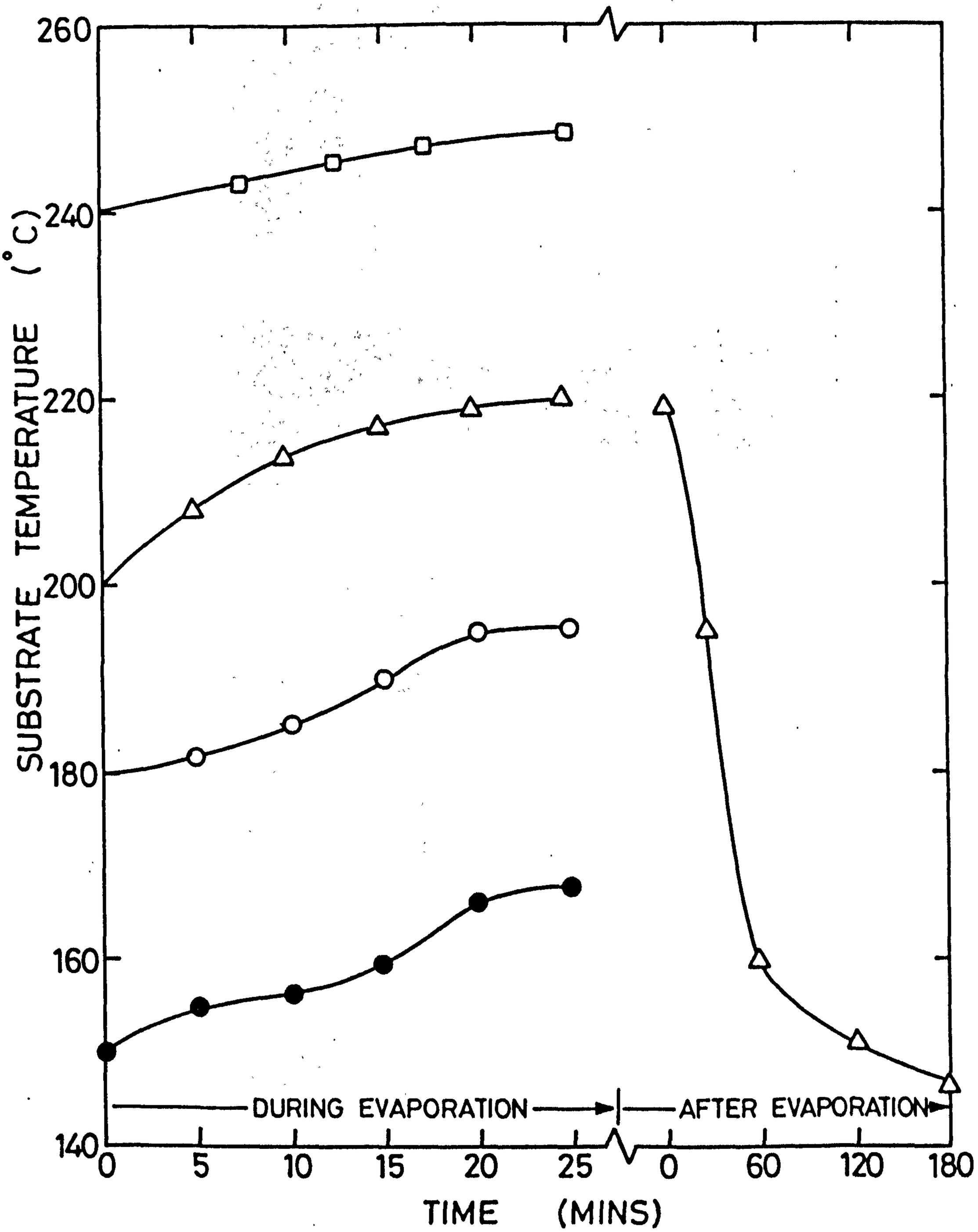
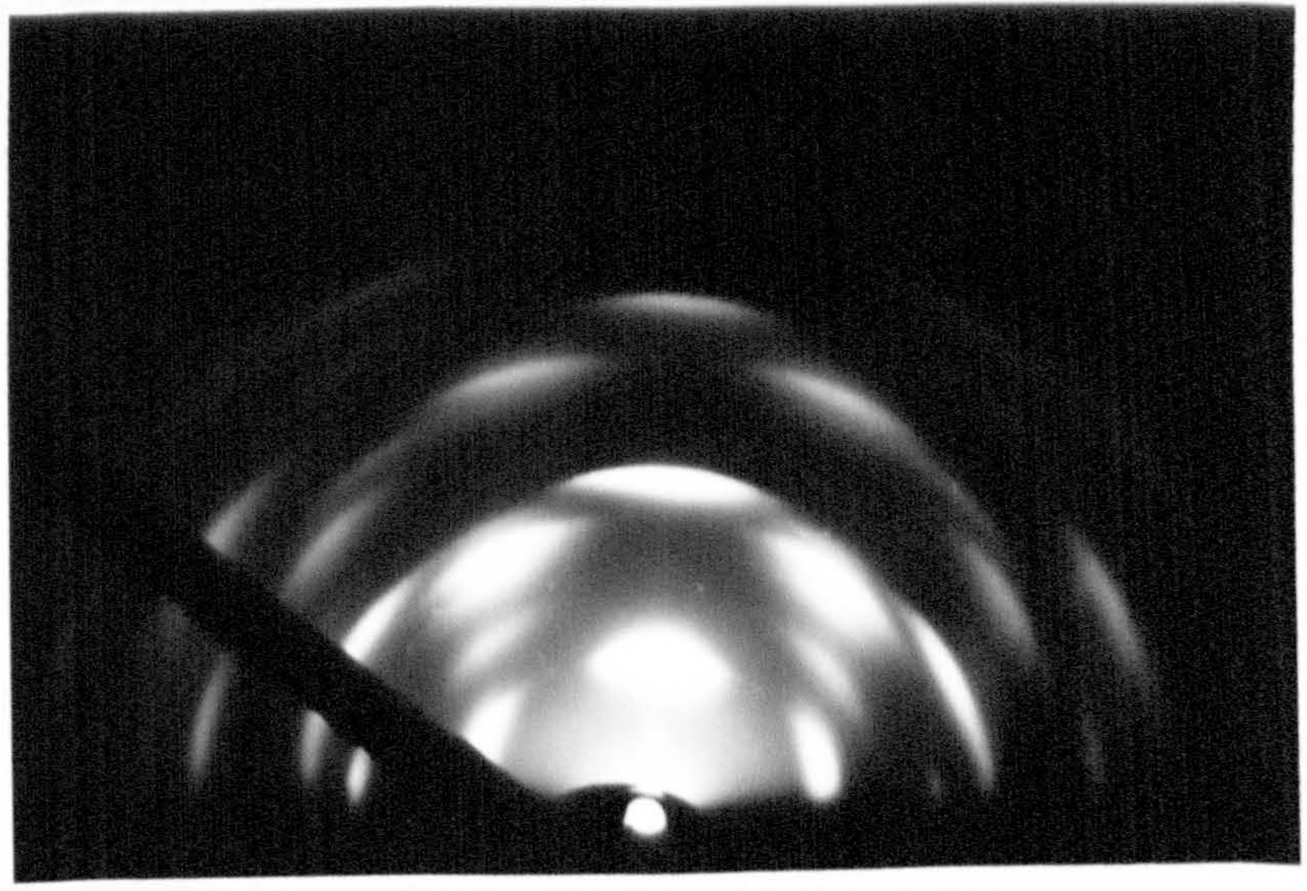
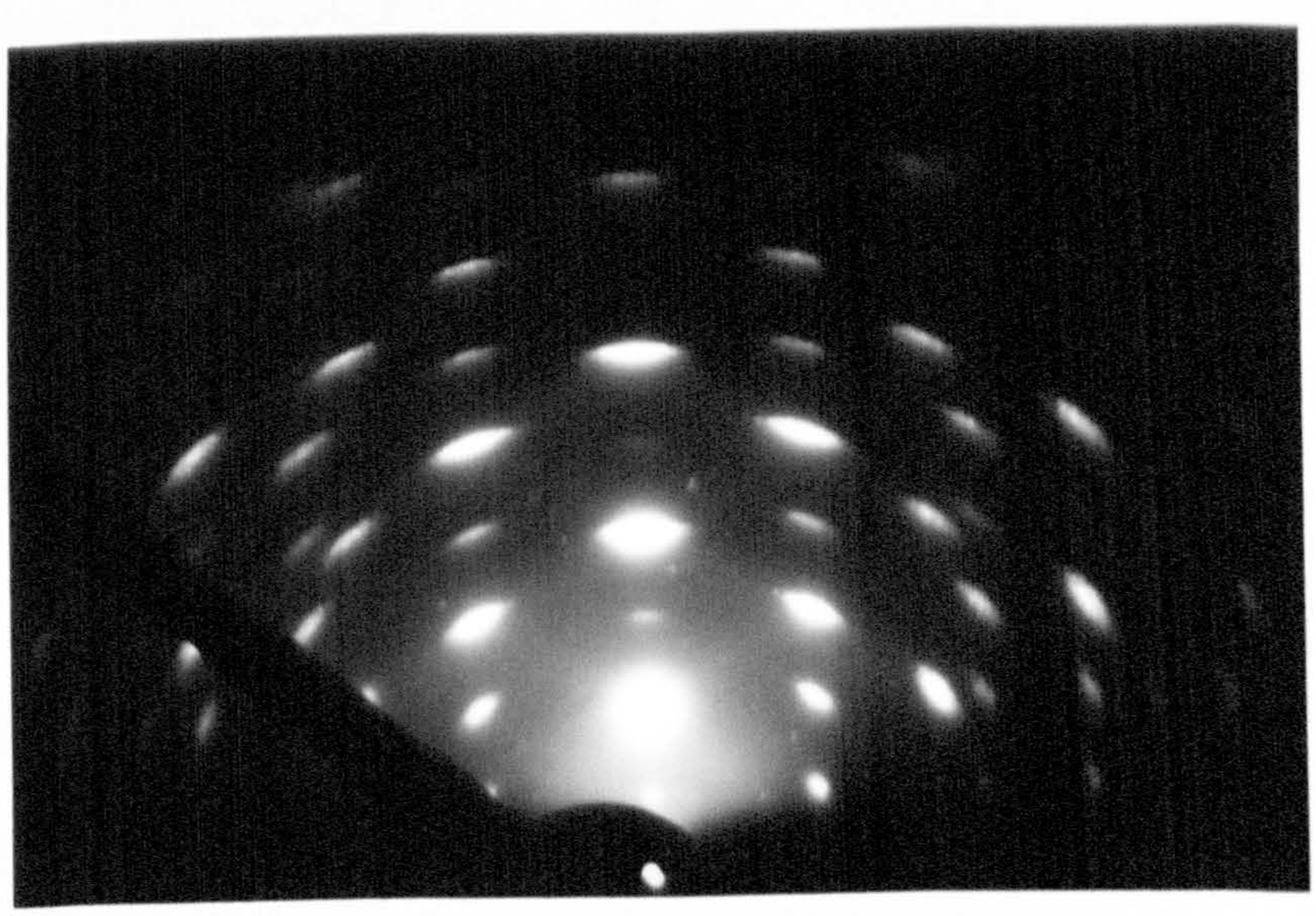


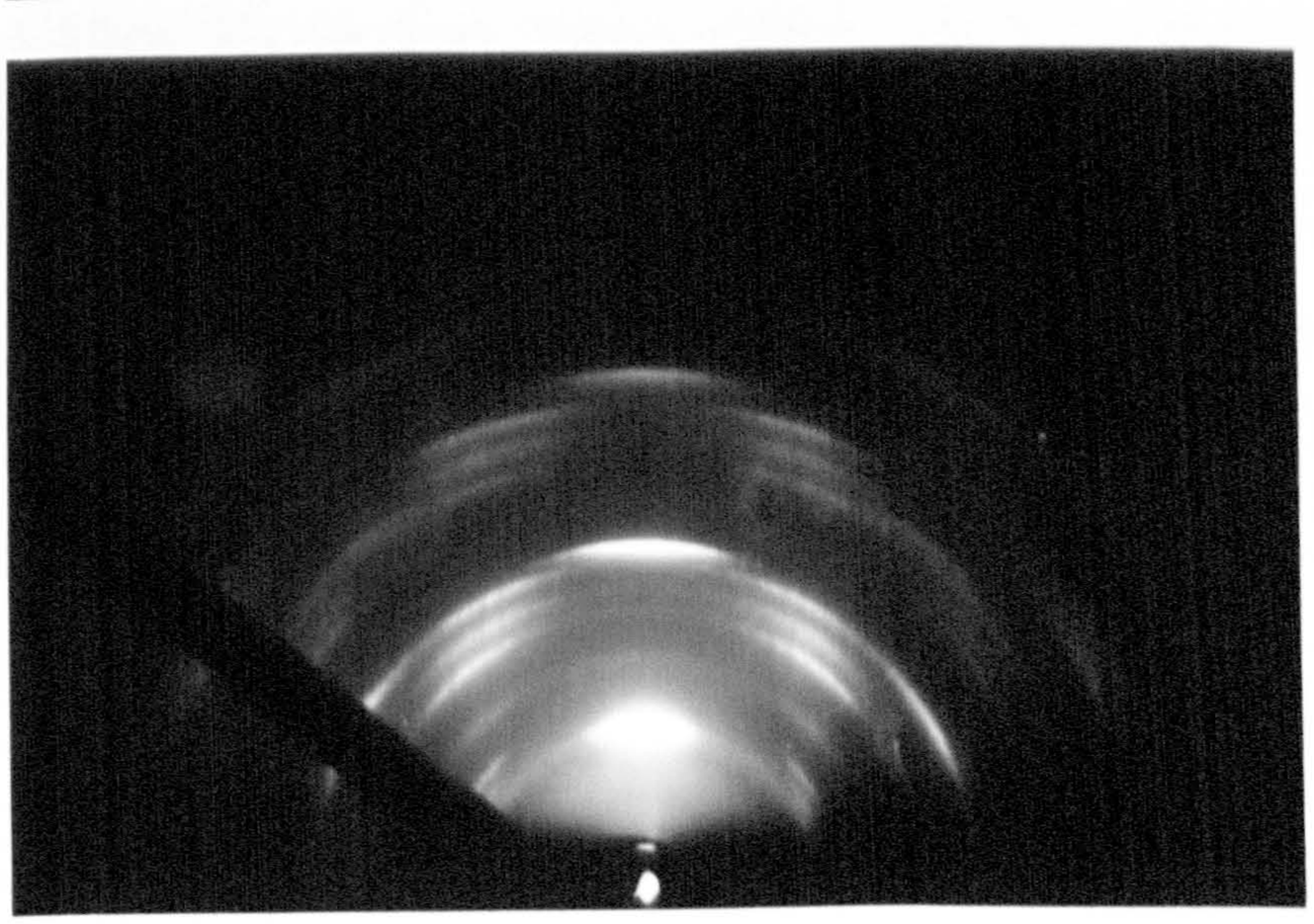
FIGURE 9.5: Measured substrate temperature during evaporation and cooling cycles



(a)



(b)



(c)

FIGURE 9.6: 100 kV RHEED patterns from three films deposited at substrate temperature (a) 150°C (b) 200°C and (c) 240°C.

150 and 240°C the patterns were characteristic of a film with a fibre axis which contains extra reflections. Similar patterns were obtained by Caswell[2] who attributed the extra reflections to the presence of two sets of crystallites which were not symmetrical about the fibre axes. One set was a mirror image about the fibre axis of the others. The RHEED pattern was indexed accordingly as shown in Fig 9.7.

It has been shown by Hirsch[3] that with crystallites with fibre axes in a [111] direction of the cubic phase or the [001] direction in the hexagonal phase, there are two low index directions in the plane perpendicular to the fibre axes corresponding to densely packed planes in real space. The two lowest index directions for the cubic phase are [110] and [211], and [120] and [100] for the hexagonal form. It was shown that the reflections from the [211] (cubic) zone coincide with those from the [120] hexagonal zone. The extra reflection exhibiting the "streak" effect perpendicular to the sample surface (Fig 9.6a and c) can be attributed to the sphalerite crystallites with two different [110] type zone axes as indicated in the indexed pattern (Fig 9.7). Once again it can be seen from Figs 9.6a and 9.7 that in the film grown at 150°C, the main reflections are due to hexagonal crystallites, although additional weak reflections from cubic crystallites also appear. The film grown at 200°C has a maximum hexagonal component while the film grown at 240°C with the intense twin reflections again suggests an increasing content of cubic sphalerite crystallites.

The SE micrographs of the fractured edge of these films deposited under various conditions are shown in the composite Fig 9.8. It is obvious that there was a progressive increase in columnar growth as T_S was increased from 150 to 200°C. In these figures those films have been compared which were grown at the same deposition rate (1.25 μm/min) and were equally thick (~ 20 μm). Two films 5 μm thick grown at 200 and 240°C are compared in Fig 9.9. It is clear that in this thickness range the columnar growth

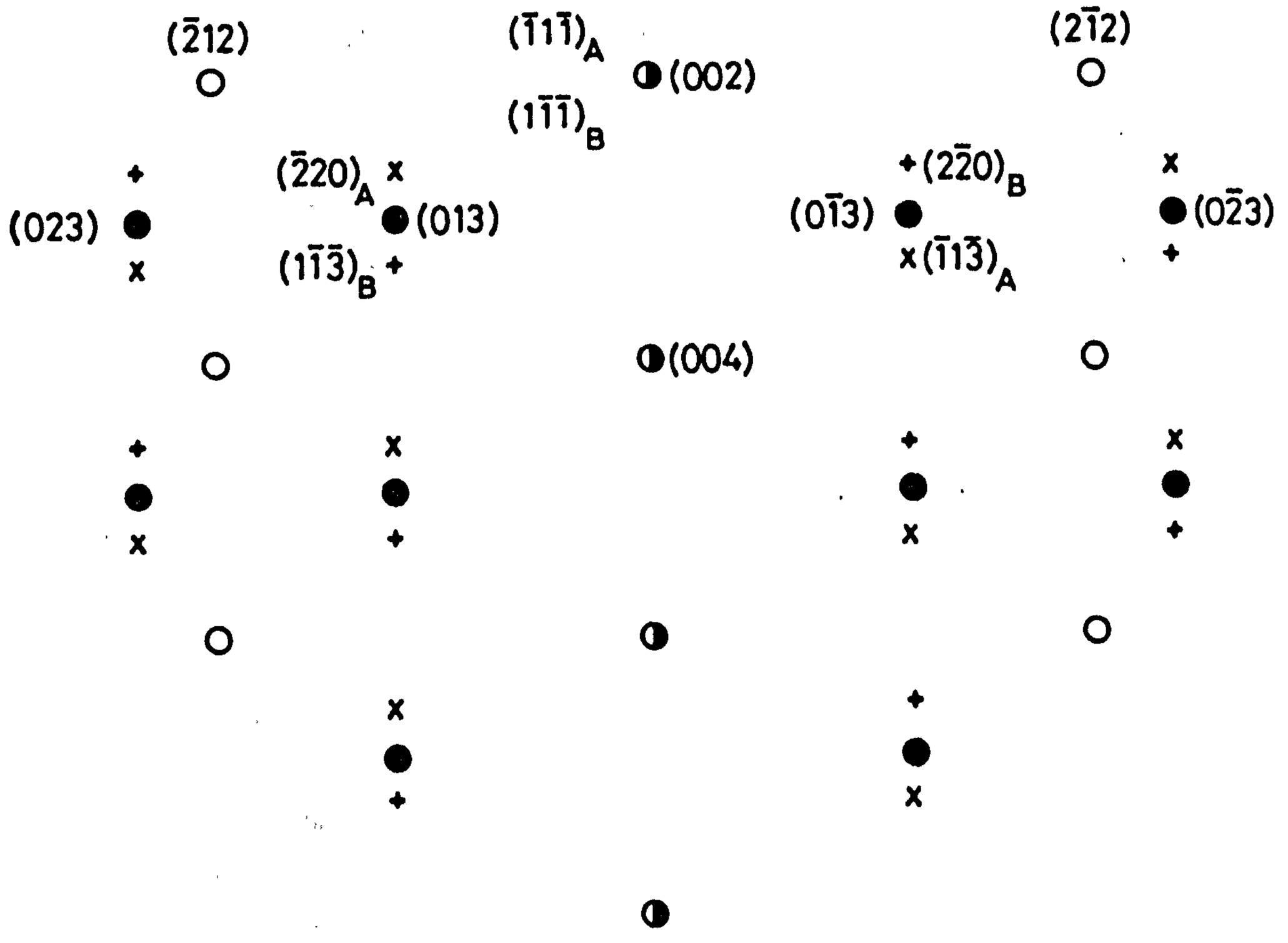


FIGURE 9.7: The indexing of the RHEED pattern shown in Figure 9.6(c)

○ (h k l) = reflection from the wurtzite phase for [120] zone axis (coincident with sphalerite [211] zone axis)

● (h k l) = reflection from the wurtzite phase for [100] zone axis

× $(h\ k\ l)_A$ = reflection from the sphalerite phase for [110] zone axis with $[\bar{1}\bar{1}\bar{1}]$ fibre axis

\+ $(h\ k\ l)_B$ = relfection from the sphalerite phase for [110] zone axis with $[\bar{1}1\bar{1}]$ fibre axis

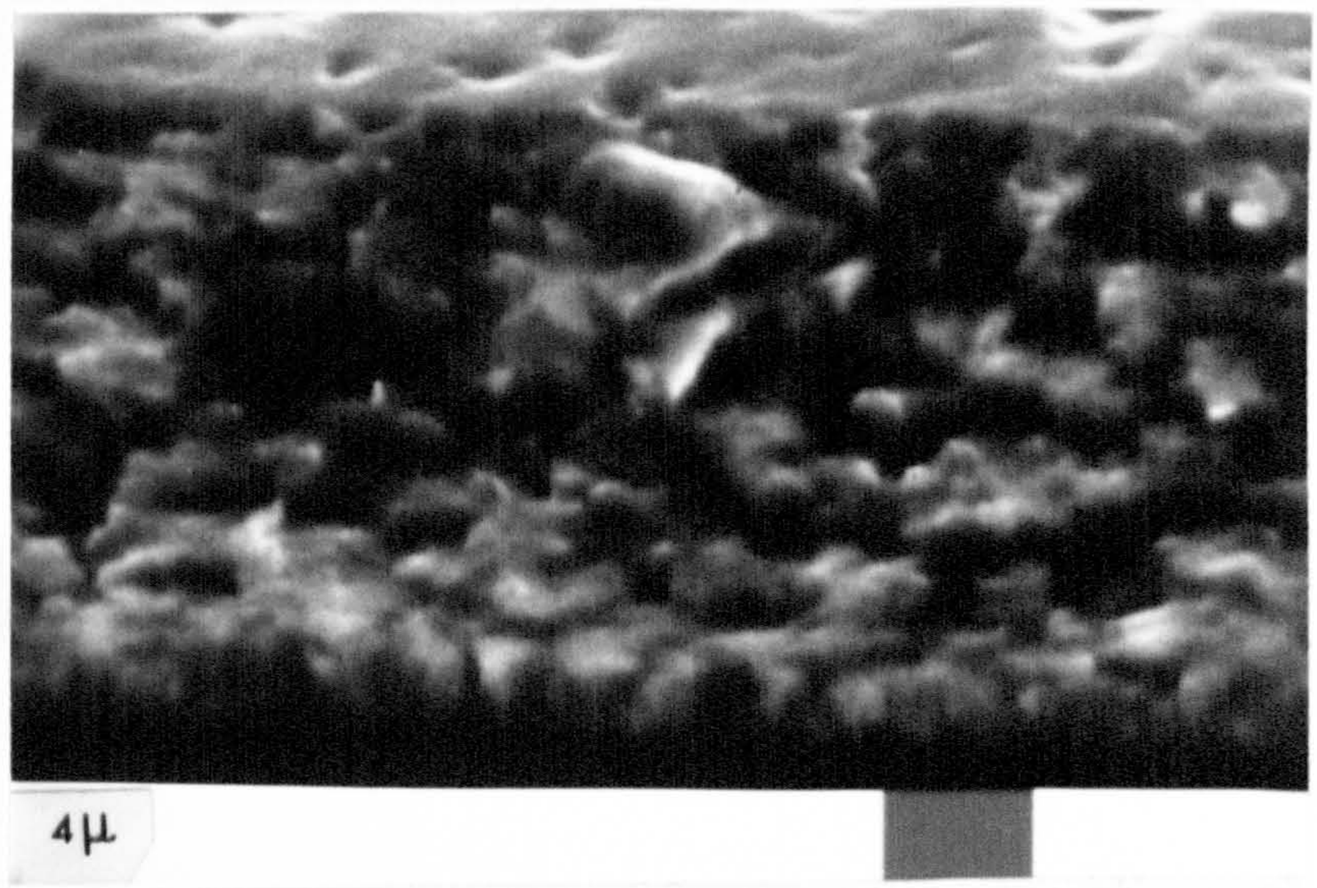
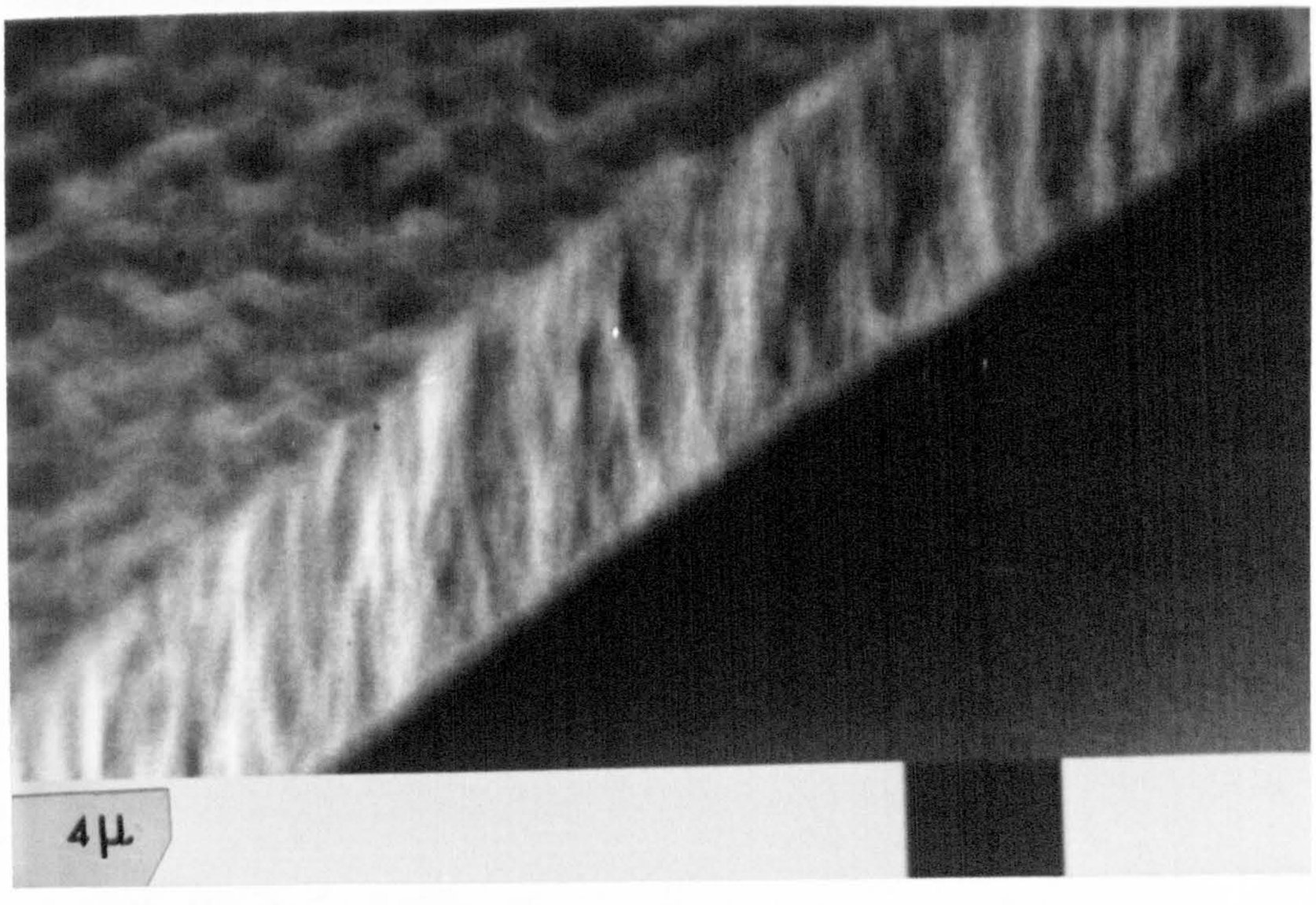
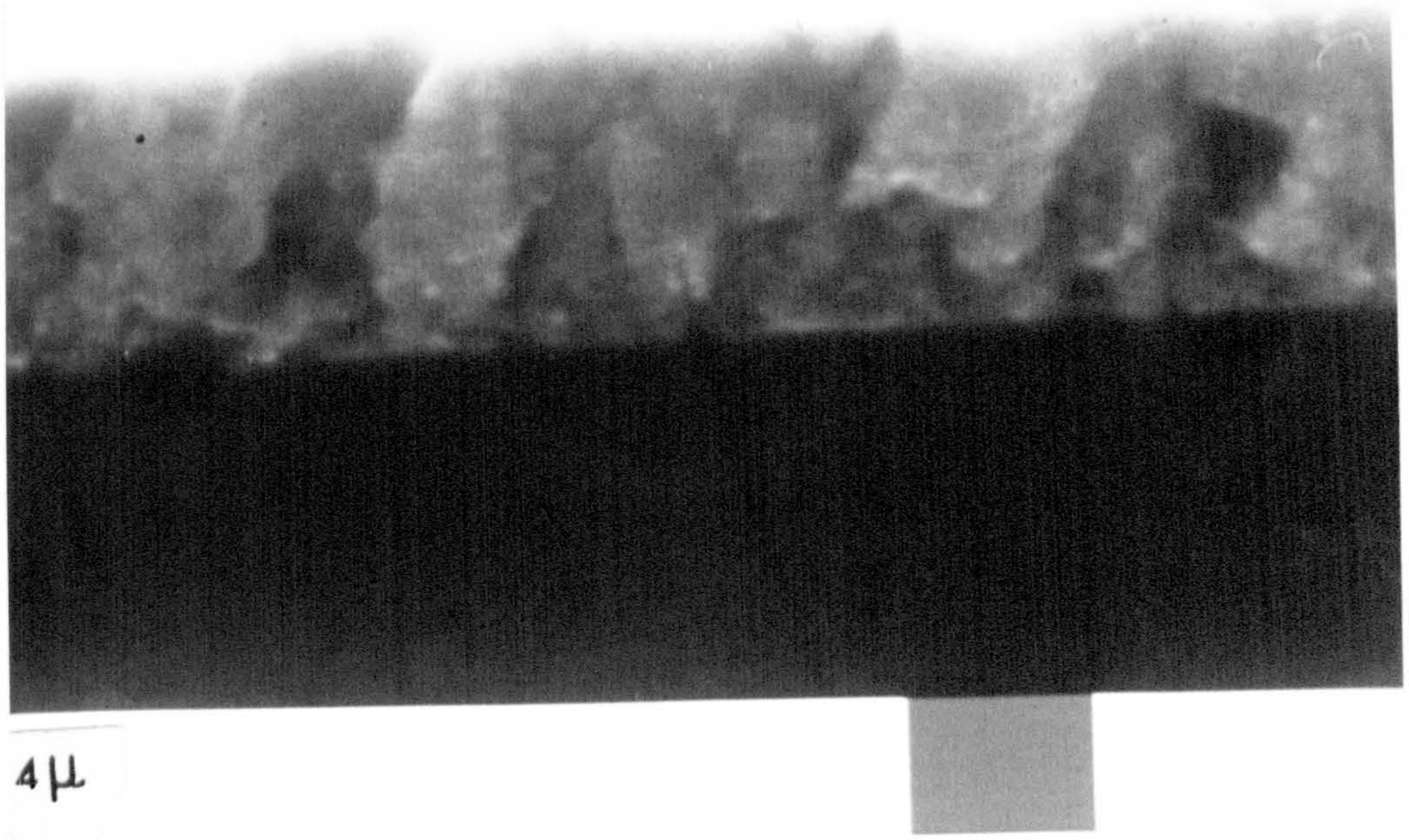


FIGURE 9.8: S. E. Micrographs of the fractured edges of films deposited at (a) 150°C (b) 180°C and (c) 200°C



(a)



(b)

FIGURE 9.9: S.E. Micrographs of films deposited at (a) 200°C and 240° C.

deteriorated as the T_S was increased beyond 200°C, though the grain size looked larger. The grain size also seemed to increase with increasing thickness comparing the two Figs 9.8 and 9.9 for the films grown at 200°C. EDAX examination of the films suggested that those grown at lower temperature had more cadmium compared with those which were grown at higher temperatures.

9.4 ELECTRICAL PROPERTIES

The effects of the variation of T_S on the electrical properties of the films deposited at a rate of 0.65 μm/min are summarized in Table 9.1.

TABLE 9.1: Effect of Substrate Temperature on the Electrical Properties of the Film.

Substrate Temp. °C	Thickness μm	Resistivity ohm-cm	$N_D - N_A$ cm^{-3}	Mobility μ $cm^2 V^{-1} s^{-1}$
150	10	50	9.6×10^{16}	1.3
180	10	200	5×10^{15}	6.25
200	10	600	1.75×10^{15}	5.95
240	5	1000	1.25×10^{15}	5

The values of the uncompensated donor density were determined from C^{-2} -V plots, and μ was determined by assuming $\mu = |(N_D-N_A)\, e\rho|^{-1}$. From this table it is obvious that the conductivity of the films decreased with increasing T_S while the mobility of the film increased initially. The difference in the mobilities of the films grown at 150°C and 180°C was quite significant. With further increases in T_S there was a slight fall in the mobility. Another noticeable feature is the decrease in (N_D-N_A) with increasing T_S. When good columnar growth was obtained at the same evaporation rate, and with a substrate temperature of 200°C, the resistivity of the film was 600 Ω-cm. Since a faster rate of evaporation has been reported to

reduce the resistivity [4,5,6], the effect of increasing the evaporation rate was studied. The results are shown in Table 9.2.

TABLE 9.2: Effect of Evaporation Rate on the Film Properties

Substrate Temp. 200°C			Thickness of films 20 μm	
Crucible Temp.	Evaporation Rate μm min^{-1}	Resistivity(ρ) ohm - cm	$(N_D - N_A)$ cm^{-3}	Mobility μ $cm^2\ V^{-1}\ s^{-1}$
730	0.2	900	1.1×10^{15}	6.3
800	0.65	580	2×10^{15}	5.38
920	0.9	200	3.75×10^{15}	8.33
1050	1.25	20	2.7×10^{16}	11.57

The resistivity clearly decreased progressively as the evaporation rate was increased. The resistivity of the film was 900 Ω cm at a deposition rate of 0.2 μm/min, and this was reduced to 20 Ω-cm when an evaporation rate of 1.25 μm/min was used. It is also obvious from Table 9.2 that the values of $(N_D - N_A)$ and of the mobility increased with evaporation rate, although there was hardly any change in the structure. It was interesting to observe that with those films in which Hall measurements were made, the values of mobility were close to those which were calculated from the measured values of resistivity and $(N_D - N_A)$.

9.5 PHOTOCAPACITANCE STUDIES

The steady state photocapacitance spectra (at 85K) of Schottky devices formed on films prepared under different conditions are shown in Fig 9.10. The four curves (a,b,c,d) are the most distinctive of the photo-capacitance spectra obtained and are representative of the films grown under

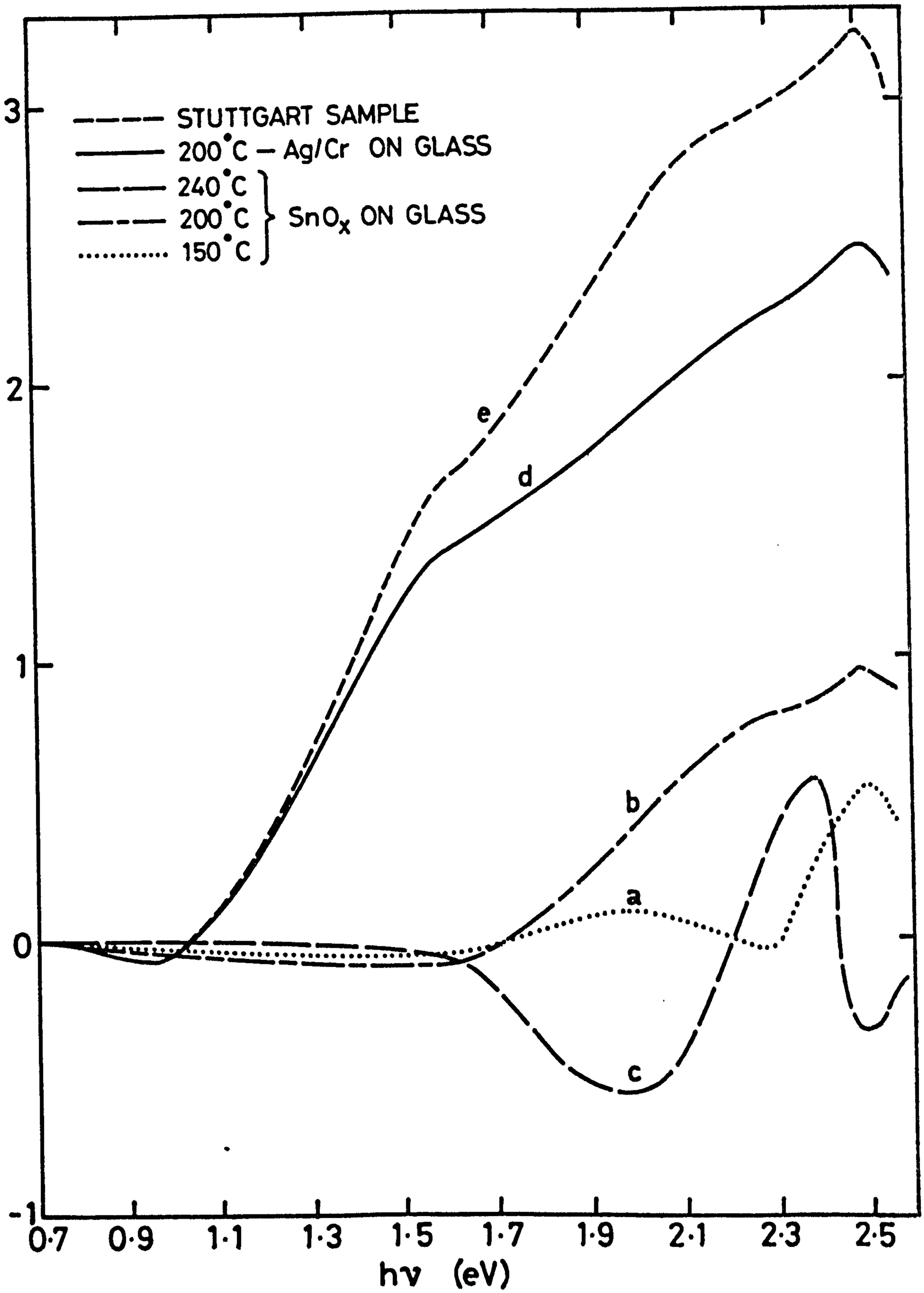


FIGURE 9.10: Photocapacitance spectra of Schottky devices formed on CdS films deposited on different substrates (SnO_x or Ag/Cr coated glass) at various temperatures.

four different conditions. Curves a,b and c are for films prepared at 150, 200 and 240°C. These films were grown on SnO_x coated glass. Curve d is for a device formed on film which was produced on Ag/Cr coated glass at 200°C.

Curve c shows that the device formed on the film grown at T_S=240°C had negative thresholds at 1.64 eV and 2.36 eV, while the onset of the enhancement of photocapacitance (ΔC + Ve) occurred at 2.05 eV and 2.48 eV. Curve b shows positive thresholds at 1.58 eV and 2.3 eV while slight quenching was observed in the infrared region. In curve a there were enhancements at 1.58 eV and 2.3 eV while a negative threshold occurred at 2.0 eV. The photocapacitance of the device formed on films prepared on Ag/Cr coated glass (curve d) gave an absolutely different pattern. After a small fall beginning at about 0.7 eV a pronounced enhancement was observed at 0.946 eV with shoulders at 1.5 eV and 2.3 eV and a final collapse at 2.48 eV.

As explained in the previous chapter, rise and fall in the photocapacitance can be explained in terms of excitation of electrons from a discrete level to the conduction band or the excitation of electrons from the valence band to such a discrete level. The curves in Figure 9.10 show that with films prepared at 240°C the dominant centre has a level 0.84eV below the conduction band. The behaviour of this centre appears to be unusual because if the negative threshold at 1.64 eV is attributed to the excitation of electrons from the valence band to this centre, then an enhancement would have been expected at 0.84 eV corresponding to the emptying of the centre to the conduction band and this was not observed. A trap at 0.84 was found by Nicholas and Woods[7] in CdS single crystals which was reported to behave in an unusual way. Moreover the rise at 2.05 eV and fall at 2.38 eV shows the presence of an acceptor-like state lying 0.43 eV above the valence band, and a donor-like state 0.12 eV below the conduction band. The acceptor may be thought to be a manifestation of excess sulphur present in the film grown at

high T_S. However, the trap at 0.12 eV below the conduction band may be a surface trap which might have formed during the cooling. Such shallow traps have been observed by Balabanov[8] during photoactivation and quenching of surface photocurrent experiments.

The spectrum of the device formed on film prepared at 200°C (curve b) is more normal in that it has a positive threshold at 1.58 eV and a small negative at 1.0 eV. This can be attributed to the capturing and excitation of electrons at the cadmium vacancy centre. Such native defects are expected in thin films and invariably occur at 1.0 eV above the valence band[9].

In curve a for the film prepared at 150° C the rise at 1.58 eV is smaller compared to curve b which indicates fewer Cd vacancies in these films grown at a lower temperature. A negative threshold at 2.0 eV suggests the presence of a deep trap 0.48 eV below the conduction band. Since the films grown at lower temperature were found to contain less sulphur, this donor may be attributed to sulphur vacancies. Traps lying at about 0.4 eV or more below the conduction band have been reported by many workers[7,10,11,12,13].

The positive threshold at 0.946 eV in the films prepared on the Ag/Cr substrate can be attributed to the presence of a deep trap at about 0.946 eV below the conduction band. The shoulder at 1.58 eV corresponds to the normal feature which it is suggested is associated with Cd vacancies. In fact this shoulder,following such a sharp rise in photocapacitance, can be interpreted as the superposition of two competing processes (i) the filling of the trap lying 0.95 eV below the conduction band, (ii) the emptying of levels due to cadmium vacancies $\sim$ 1.0 eV above the valence band. It is interesting to note that exactly similar spectra were obtained with the devices formed on CdS films deposited at the Stuttgart laboratory (Fig 9.10). Those films were also grown on the Ag/Cr coated glass. It is therefore suggested that during the deposition of CdS, silver diffuses in CdS[14] to form a complex with Cd vacancies.

9.6 HETEROJUNCTION CHARACTERISTICS

Typical J-V characteristics of heterojunctions formed on the films grown at 150°C and 200°C are shown in Fig 9.11. The most obvious difference between these curves is the better fill factor of the device formed on the film put down at 200° C. It was shown in section 9.3 that the films grown at 200°C had a much better developed columnar structure, and this evidently improves the fill factor.

The values of the OCV and SCC also varied with the growth conditions, (see Fig 9.12). Here it is obvious that the OCV obtainable, increased from 0.4 to 0.49V as T_S was increased from 150 to 200°C. The SCC also increased from 8.5 to 10.5 mA/cm^2. With the devices formed on films grown with T_S above 200°C the OCV decreased slightly, but the SCC collapsed dramatically. The measured current-densities were not particularly large because no attempt was made to provide a proper grid arrangement for current collection. The performance of cells formed on films produced at Stuttgart was also compared with the Durham devices. The OCV, SCC and FF obtained using a Stuttgart film were 0.52 V, 15 mA/cm^2 and 0.6 while with Durham films (Ag/Cr substrate) the corresponding results were 0.5V, 12 mA/cm^2 and 0.57.

The spectral responses of the OCV of the various devices are compared in Fig 9.13. Two peaks at 0.96 μm and 0.7 μm appeared when the film had been grown at 150°C. With T_{200} substrate the dominant peak in the response occurred at 0.96 μm, while with higher substrate temperatures the relative magnitude of the 0.78 μm peak increased. These measurements were carried out both at R.T and L.N temperatures and to avoid confusion the low temperature responses are shown in Fig 9.13. Following the work on single crystal devices the peaks at 0.96 μm and 0.78 μm are taken to be associated with the chalcocite and djurleite phases of Cu_xS. This assignment suggests that the phase of the Cu_xS on the films prepared at the lower substrate temperature is a mixture of chalcocite and djurleite. Some digenite might also be formed if

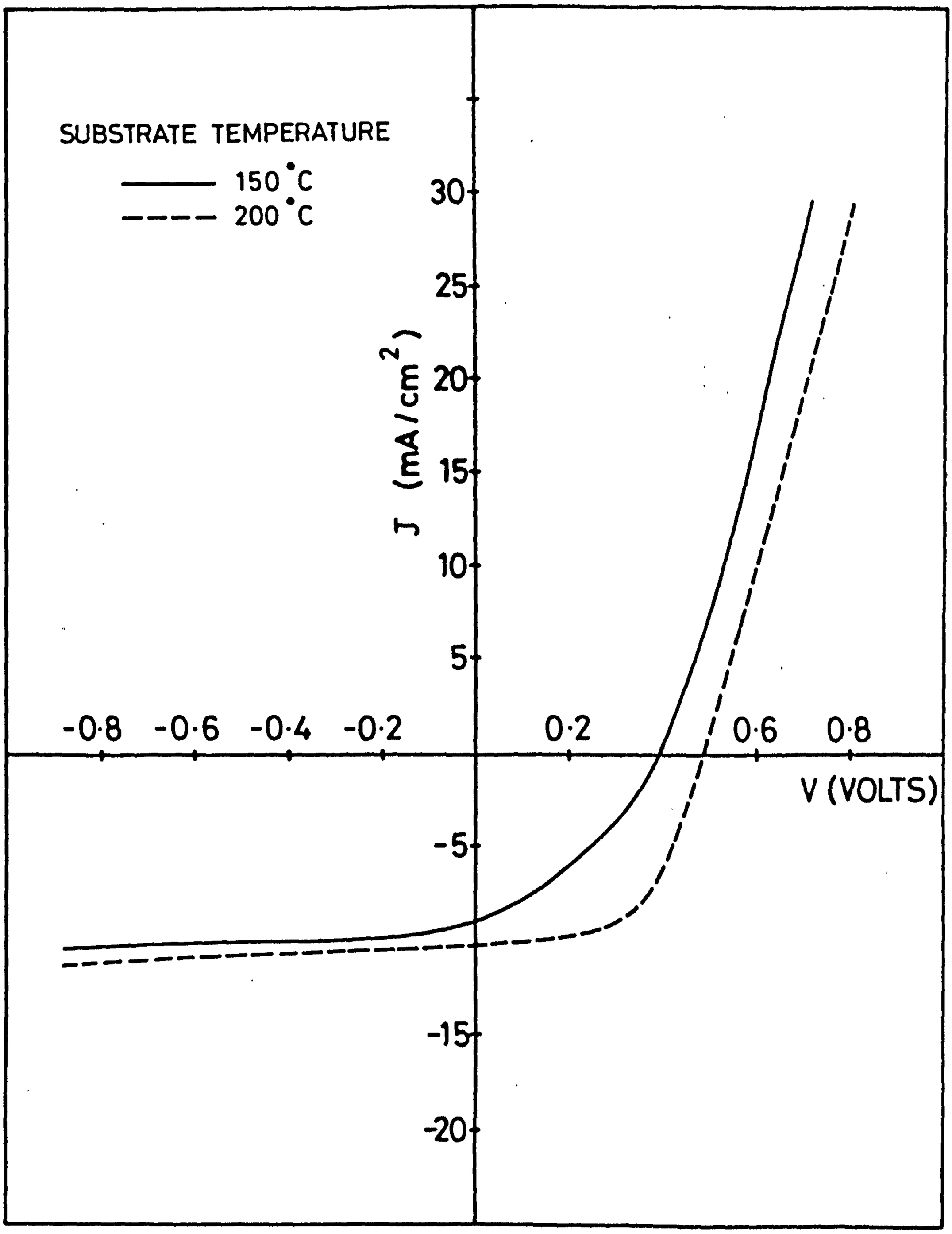


FIGURE 9.11: Current voltage characteristics (under AM 1 illumination) of heterojunctions formed on films deposited at 150°C and 200°C.

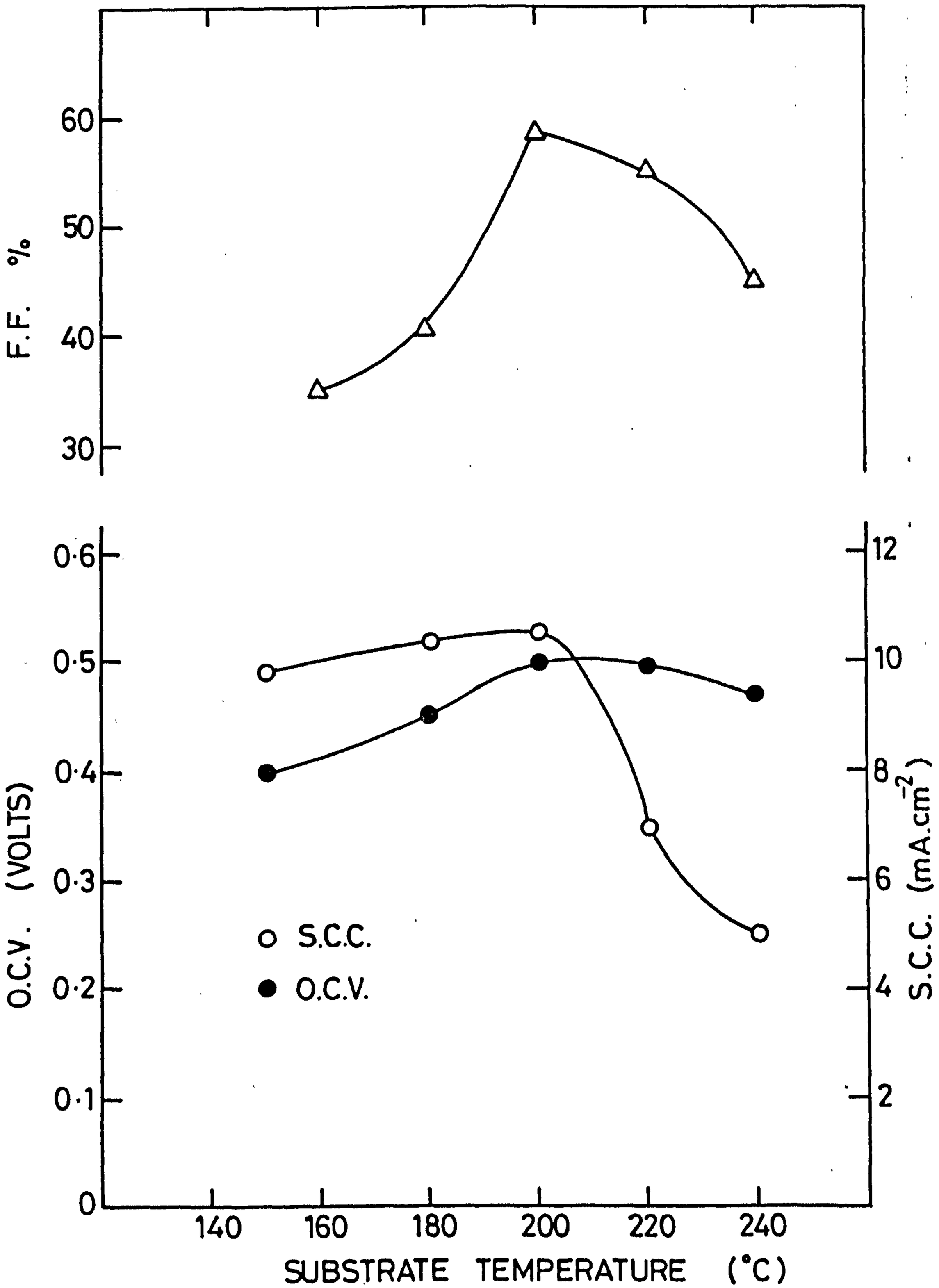


FIGURE 9.12: The effect of substrate temperature used during the deposition of CdS films on the device parameters.

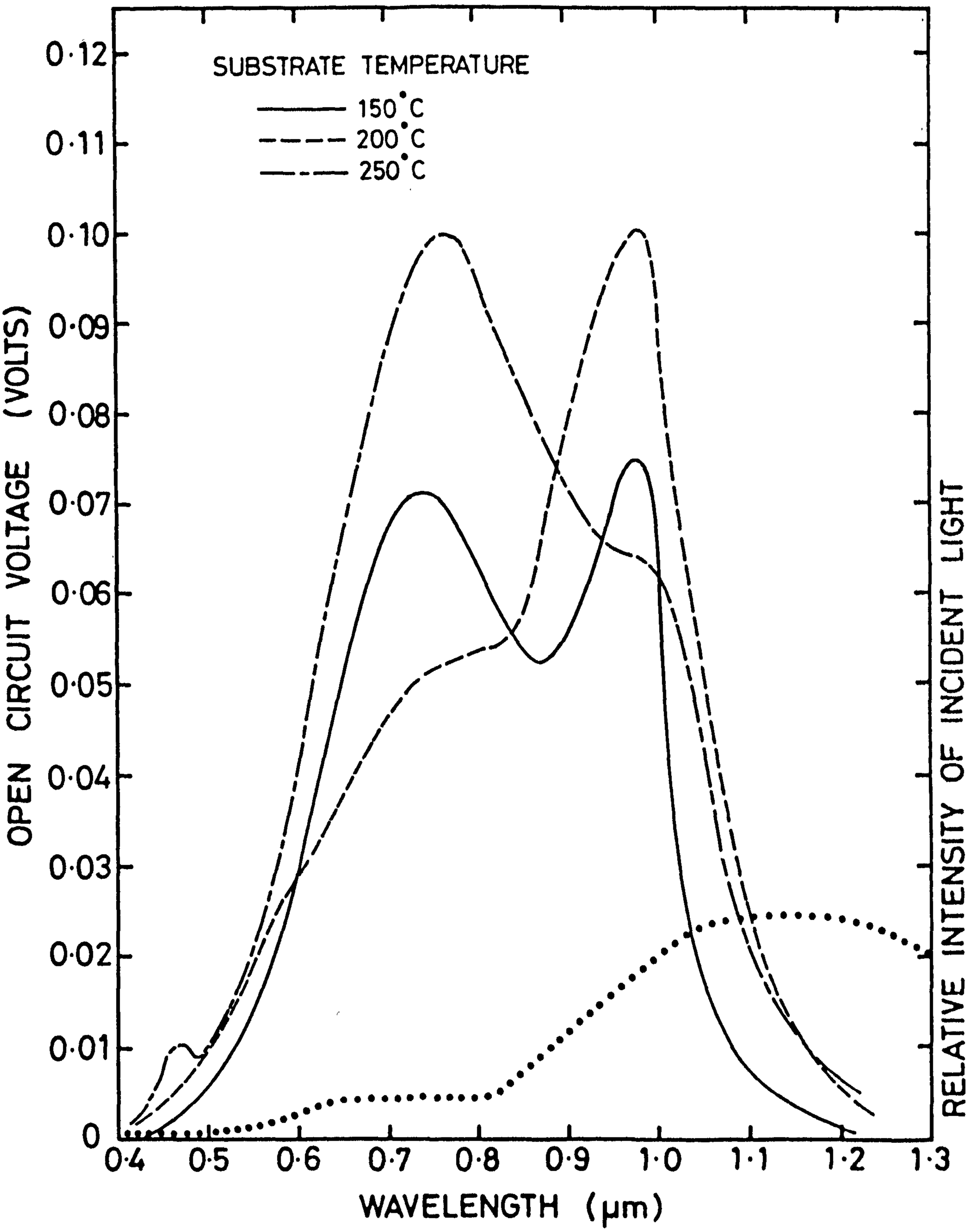


FIGURE 9.13: The spectral responses of the OCV (measured at 85K) of as-prepared devices formed on films deposited at different temperatures on SnO_x coated glass.

the CdS layer contains some cubic phase material. Copper sulphide films formed on CdS layers grown at 200°C have better stoichiometry and the chalcocite is formed. Further increase in T_S during the deposition of the CdS films increases the cubic component as well as the sulphur content. Both the factors affect the phase of Cu_xS adversely. A slight excess of cadmium has been found to be beneficial in the thin film devices formed by the dry barrier process[15].

As mentioned earlier any device must be given a post preparative heat treatment to improve its efficiency. The spectral responses of some heated devices are shown in Figure 9.14. The diffusion of copper in CdS on SnO_x coated glass is obvious from the response at 0.65 μm (Section 5.3.1). It is interesting to note that the response of devices on films on Ag/Cr indicates a minimum diffusion of copper. The major peak was at 0.96 μm even after heat treatment. When these measurements were made at L.N. temperature the peak at 0.65 μm shifted to 0.78 μm indicating the presence of djurleite (Fig 9.15).

The photocapacitance spectra of heterojunctions formed on films deposited on SnO_x and Ag/Cr coated glass are compared in Fig 9.16. The infrared quenching of photocapacitance of devices on SnO_x coated glass was similar to that of devices on single crystals, although the percentage quenching was less (curves a and b). A major difference was found with the device on films on Ag/Cr coated glass (curves c and d). At R.T. a quenching in the photocapacitance was observed at 0.78 eV which was followed by a sharp rise (ΔC + ve) at 0.96 eV. At L.N. temperature the quenching at 0.78 eV disappeared and the spectrum was dominated by the enhancement in photocapacitance with a threshold at 0.946 eV. The photocapacitance changes in thin films on SnO_x coated glass can be explained in terms of a copper level with ground and excited hole energies of 1.1 and 0.35 eV above the valence band (Section 6.2). However, with cells on Ag/Cr coated glass the presence of the trap 0.946 eV

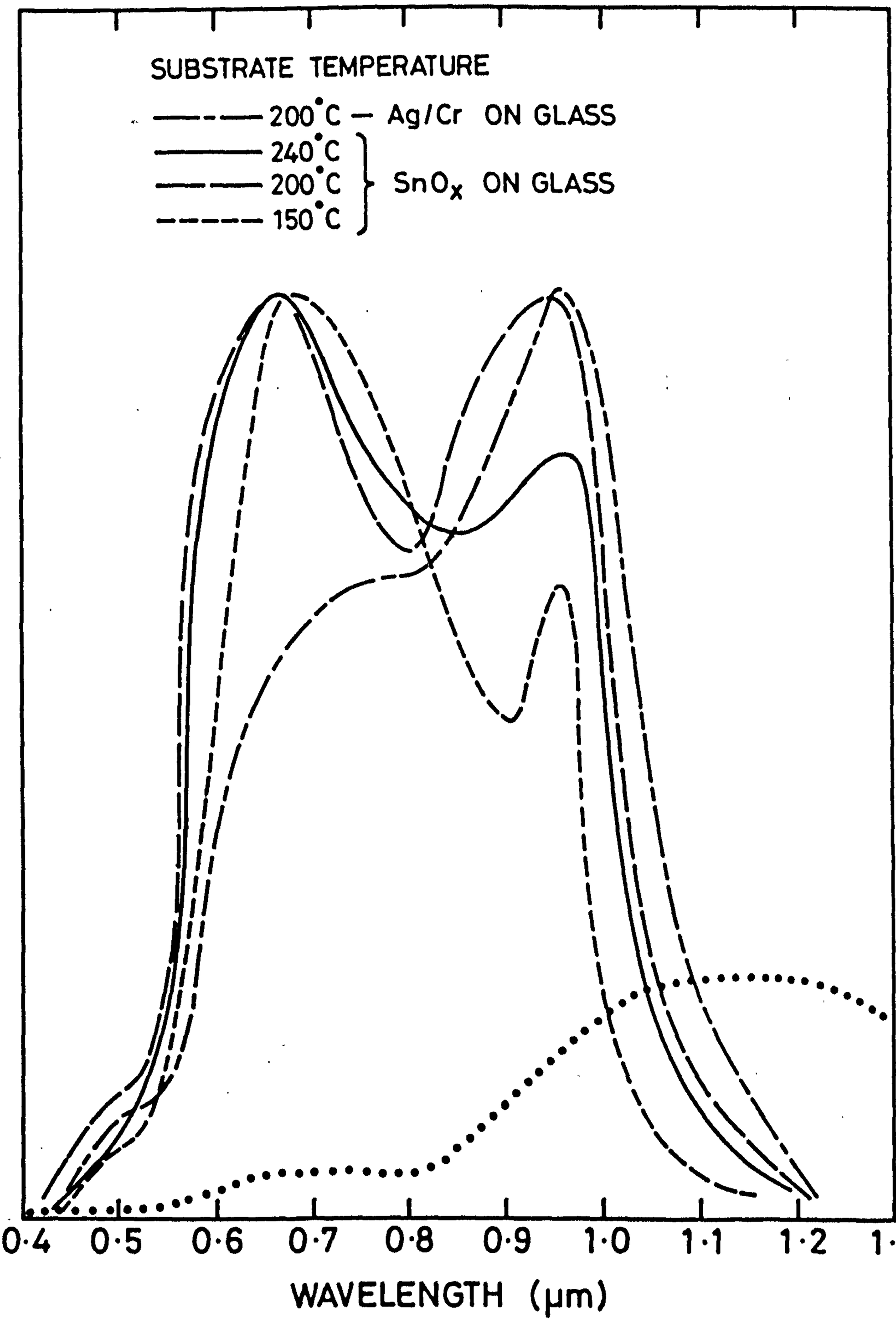


FIGURE 9.14: Spectral responses (measured at 295K) after a post barrier heat treatment of heterojunctions formed on films deposited on different substrates at various temperatures.

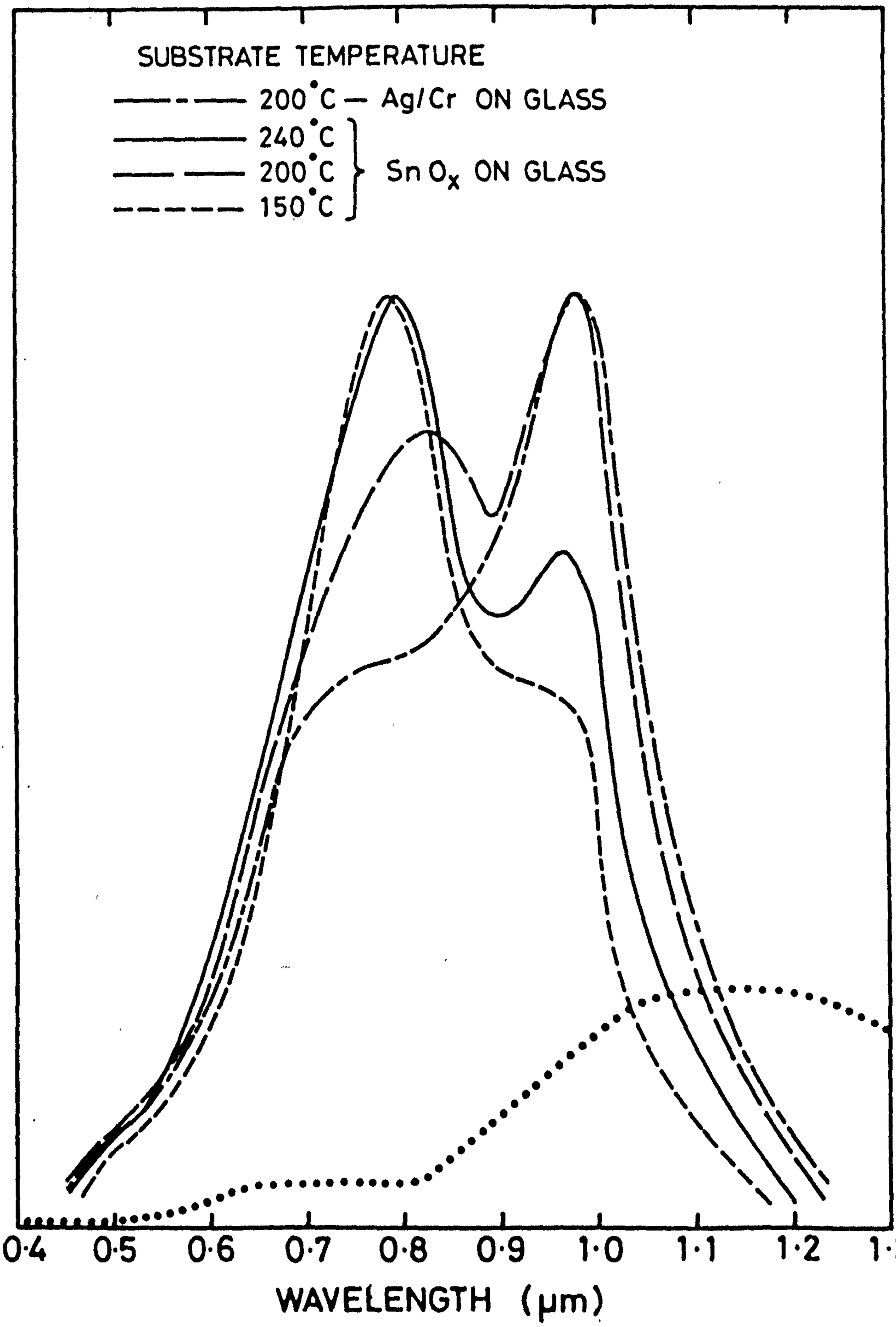


FIGURE 9.15: Spectral responses of devices as in Fig 9.14 but measured at 85K.

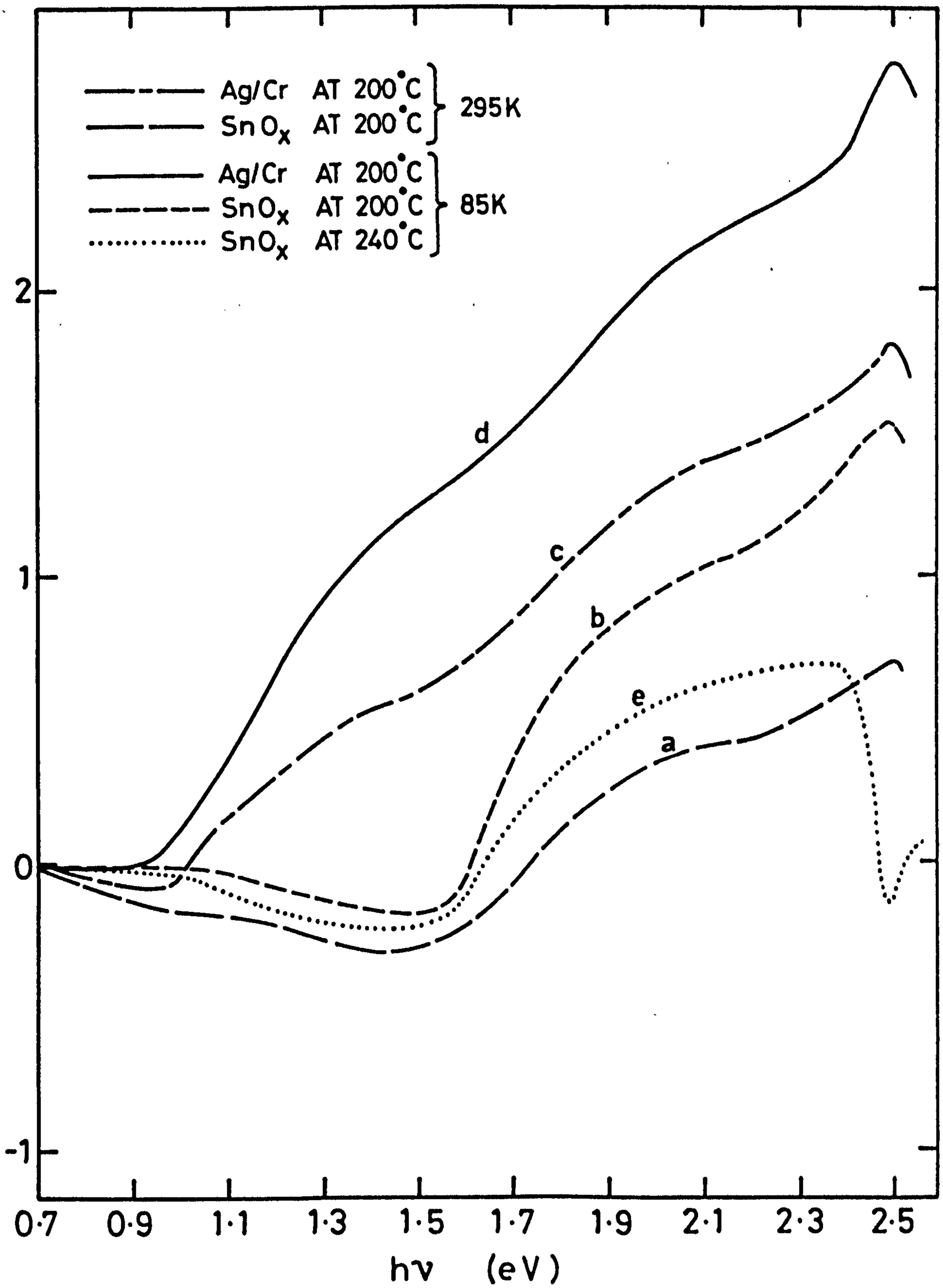


FIGURE 9.16: Photocapacitance spectra of heterojunctions formed on films deposited on SnO_x and Ag/Cr coated glass.

below the conduction band seems to inhibit the copper diffusion in the CdS so that the pronounced positive going signal at 0.946 eV appears as electrons are excited from this trap to the conduction band. At the same time a negative going threshold would be expected at ∿ 1.54 eV where this level was filled with electrons from the valence band. However a rise was observed in that region although a shoulder also appeared which can be attributed to the competing excitation and quenching processes. Whether this enhancement at about 1.5 eV was due to excitation of electrons from the deep acceptor formed by cadmium vacancies or substitutional copper is not clear because the two states lie so close to one another.

The excitation of the trap at ∿ 0.1 eV in the device formed on the film deposited at 240°C is quite obvious from the sharp quenching at 2.38 eV (curve e). Otherwise the spectrum shows the normal infrared quenching and excitation at 1.58 eV which corresponds to copper levels.

In an attempt to prepare junctions in an alternative way by spreading a layer of CuCl on to the CdS substrate, some interesting results were obtained. The idea was to avoid having to evaporate the CuCl. A solution of CuCl was prepared in acetonitrile which is supposed to dissolve only Cu^{I} compounds, and a small amount of propylene glycol was added to increase the viscosity. The suspension was applied to CdS single crystals and thin films which were then dried at 100°C for 10 min. The samples were then heated in argon at 200°C for 2-3 min. The photovoltaic effect was quite obvious. Typical J-V characteristics are shown in Figure 9.17. The maximum OCV and SCC on single crystals were 0.46 V and 12 mA/cm^2. The fill factor was 0.7. The values of these parameters when thin evaporated films were used were 0.4V, 8 mA/cm^2 and 0.6.

The Cu_xS phase was identified as digenite by the spotty rings in the RHEED pattern (Fig 9.18). The good agreement between the measured d spacings and values taken from the ASTM index for the more intense of the spotty rings,

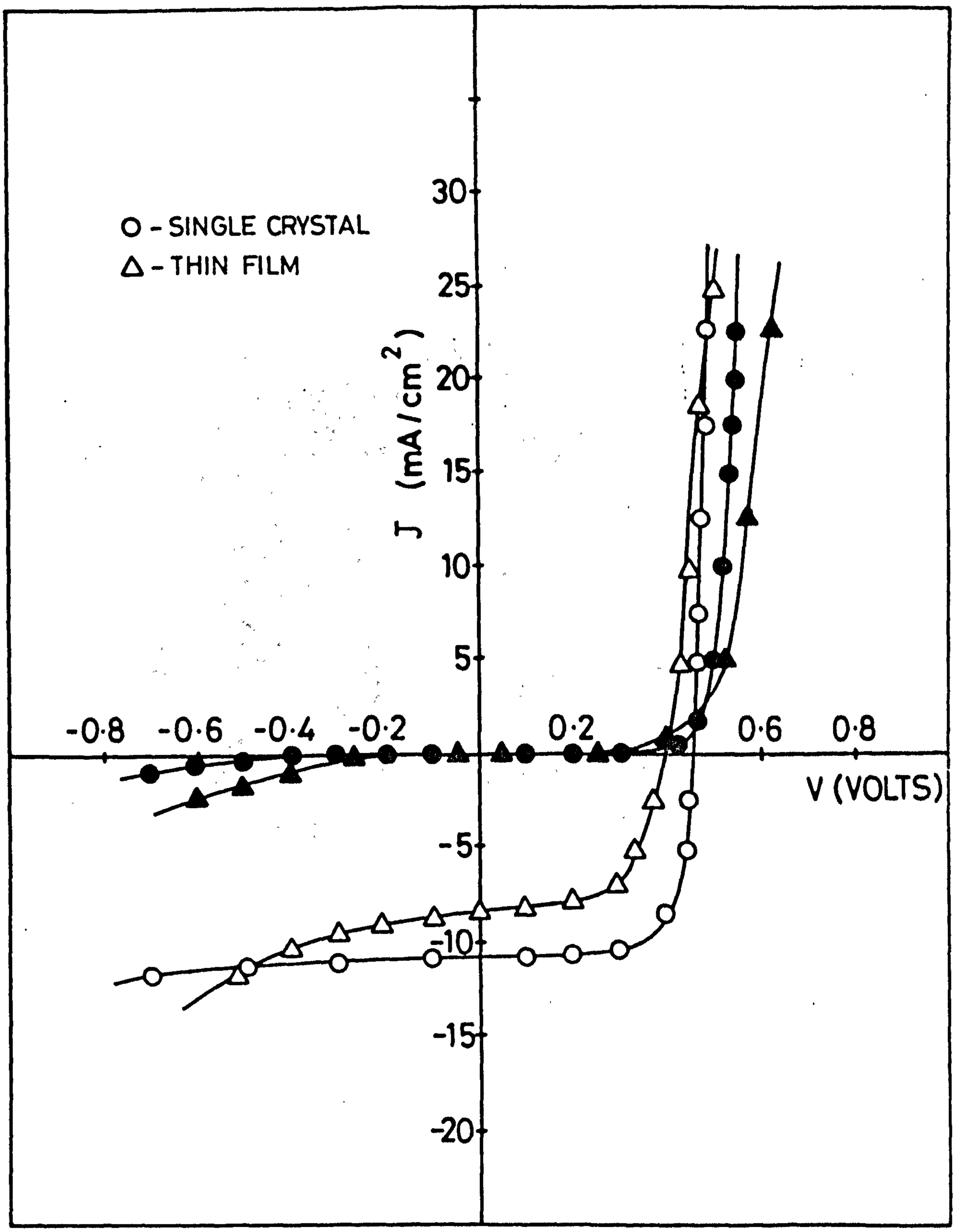


FIGURE 9.17: J-V characteristics of the heterojunctions formed by the application of a solution of acetonitrile and CuCl on CdS.

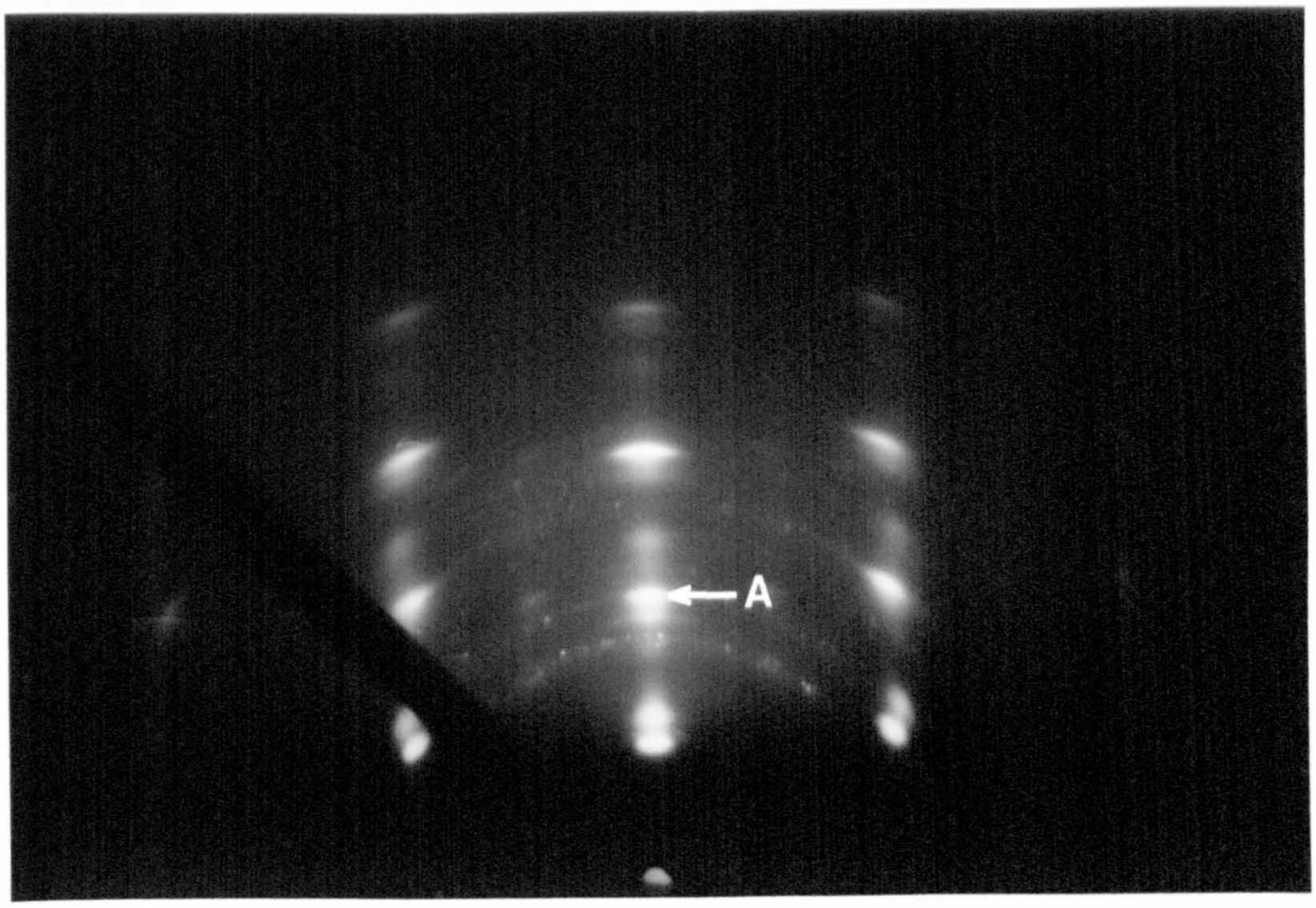


FIGURE 9.18: The RHEED pattern from the Cu_xS layer formed by spreading the solution of acetonitrile on CuCl on single crystal CdS.

shown in Table 9.3, confirm this identification.

TABLE 9.3: Measured d Spacings and ASTM Index Data for Digenite

Measured Values		A.S.T.M.Data	
d values A^{o}	Estimated Intensity	d values A^{o}	Intensity (hkl) (%)
3.30	weak	3.21	40 5 5 5
2.05	strong	1.975	100 0 10 10
1.94	strong	1.686	30 5 5 15
1.33	strong	1.33	10 0 0 20
1.10	strong	1.13	20 10 10 20

A number of the spotty rings appeared to coincide with the strong spots in this pattern, perhaps the most interesting of these was the spot A corresponding to the (5 5 15) reflection which has a d spacing of 1.686 A^{o}. This value is very close to that of the (004) interplanar spacing of CdS which is 1.679 Å. However, attempts to index pattern A, showed that the intense diffraction spots could not be explained in terms of the (5 5 15) plane of digenite lying parallel to the (004) plane of CdS.

Though digenite is not a desirable phase of Cu_xS in the CdS-Cu_xS heterojunction, these observations show that this method of preparation on single crystals leads to agreement with the findings of Vedel et al[16] who have used thermogravimetric analysis to investigate the layer of Cu_xS formed by spraying

a solution of CuCl in acetonitrile, when a mixture of digenite and covellite was obtained.

The spectral response varied from device to device. In some, a larger response developed at 0.7 μm indicating the presence of a copper deficient phase of Cu_xS, however in some cells the peak associated with chalcocite also appeared.

9.7 DISCUSSION

Thermally evaporated films of CdS have been studied extensively by many workers[4-6,17-20] and reviewed by Stanley[21] and Hill[22]. The effects on the electrical and optical properties of varying preparational parameters of 1-5 μm thick films have been studied previously in this laboratory[23]. The present study was carried out on much thicker films (5-20 μm). One of the features of films in this range of thickness is that the evaporation rate does not affect the structure of the films. The substrate temperature is the important parameter controlling the crystallinity of the films. However, the electrical properties are a function of both substrate and source temperatures.

The growth of the CdS films by thermal evaporation is a process in which CdS dissociates into Cd and S_2 vapours[24,25] which then condense on the substrate and recombine. It has been suggested that the stable configuration of sulphur at lower temperatures is the S_8 molecule, whilst at higher temperature it is the S_2 molecule[26,27]. Therefore at lower temperatures when the recombination of Cd and S does not proceed as rapidly as the impingement rate, the unreacted S_8 species re-evaporates and the films are Cd rich. As the temperature is increased more stoichiometric CdS is formed. However, increasing T_S above 240°C assists re-evaporation so that thinner films are obtained. The surface diffusion of adsorbed particles has been found to play a decisive part in the growth mechanism[28]. The deterioration in the columnar growth and enhancement of lateral growth at 240°C may be due to the presence of increased adsorbed sulphur.

These suggestions offer an explanation of the observed electrical properties. The increase in the resistivity of the films with increasing T_S indicates an enhancement in the sulphur content, which was also observed by EDAX. Although the films grown at 150°C were much more conducting than those grown at 200°C, the mobility of the previous film was much lower. This is attributed to more pronounced intergranular particle barriers[29-31] as evidenced by the poor columnar growth.

The effect of increasing the evaporation rate in reducing the resistivity while maintaining the columnar growth is obvious from the results in Table 9.2. It is important to note that the mobility also increased. Higher evaporation rates are expected to provide more cadmium[23]. This is clearly in line with the increase in the compensated donor densities in the films deposited increasingly rapidly. Hall measurements of in plane mobility gave the same value as that derived from C-V plots and film resistivities. This suggests that the intergranular barriers limiting the mobility are the same in the lateral and longitudinal directions.

The effects of varying the preparational parameters on the structural and electrical properties were reflected in the heterojunction characteristics. The increase in the OCV when T_S was increased from 150 to 200°C can be attributed to the variation in diffusion potential due to the change in the relative position of the Fermi level as the compensated donor densities decreased[32]. The grain size would also play a contributory part. However, on increasing T_S beyond 220°C, there was a slight decrease in the OCV even though the uncompensated donor density also decreased. The photocapacitance studies revealed the presence of shallow traps 0.12 eV below the conduction band in the films grown at higher temperature. It is possible that the tunnelling of electrons through such traps reduced the barrier so that OCV decreased.

As far as the SCC of the devices is concerned, the variation would be a combined effect of the stoichiometry of the Cu_xS layer[33,34] the electrical and structural properties of CdS[15,34-38] which leads to interface recombination[9] and tunnelling processes[40,41] and the nature of the intergranular barriers[42,43]. The stoichiometry of the Cu_xS depends on the structure of the substrate[44]. The RHEED patterns indicated the presence of cubic crystallites in the films deposited at 150 and 240°C, while an excellent hexagonal pattern was obtained from the films deposited at 200°C. The spectral response of the as-prepared devices on the hexagonal substrate revealed the predominance of the chalcocite phase, while in the substrates with a mixture of cubic and hexagonal CdS, an additional peak in the spectral response indicated the presence of a copper deficient phase which might have been a mixture of djurleite and digenite[45]. Thus one of the reasons for the lower SCC in devices formed on the films deposited at 150°C and 240°C can be attributed to the presence of undesired phase of Cu_xS. This indicates the importance of producing a film with a good hexagonal structure.

A high series resistance will also reduce the SCC. This will be important for films deposited at temperatures above 220°C. The intergranular barrier would also affect the SCC. Using the expression $\mu_H = \mu_o e^{-q\phi/kT}$ where μ_o is taken to be 300 $cm^2 V^{-1} s^{-1}$ (corresponding to the values for single crystals of CdS), the intergranular potential barrier were found to be 0.08 eV high for the films deposited at 200°C. With the film deposited at 150°C the barrier height increased to 0.14 eV. These values represent two extremes and demonstrate the importance of the growth condition in determining the barrier height.

The influence of these barriers can be made more clear by considering the J-V characteristics (Fig 9.11) of the devices on films formed with T_S = 150°C. These devices had poor fill factors. Now the resistivity of the film grown at 150°C was low, so that the poor fill factor can not be

attributed to a high series resistance. According to Rothwarf[39] the deviation of the fill factor from an ideal value, $\Delta FF = FF_o - FF$, is given by

$$\Delta FF = C \frac{J_s R_s A}{V_{oc}} + \frac{V_{mp}^2}{V_{oc} J_{sc} A R_{sh}} + (\Delta FF)_{F_2}$$

Here the first term corresponds to loss due to series resistance, the second term is associated with that due to shunt resistance and the third involves the interfacial field F_2. From the slope of the J-V curve (Fig 9.11) at $V = 0$ and $V = V_{oc}$ the contribution due to series and shunt resistance seems to be comparable in the two devices, so that the reduction in the fill factor may be associated with the third factor which relates the reduction in the fill factor to the interfacial field (see Section 3.5.4) in the following way

$$(\Delta FF)_{F_2} = \frac{V_m}{V_{oc}} S_I \frac{1 - F_2(V_{mp})/F_2(o)}{S_I + \mu_2 F_2 (V_{mp})}$$

The field would be modified by the presence of the traps[39,46]. At the same time the mobility would also influence it. Thus the growth conditions used for deposition would ultimately affect the fill factor.

The importance of silver as a back contact has been discussed by Bloss and Pfisterer[47] and according to them it helps to restrict short circuiting. Our work shows that an additional trap is formed at 0.940 eV below the conduction band on devices on layers on Ag/Cr, and the trap appears to inhibit the diffusion of copper in CdS, since although heat treated devices formed on films on SnO_x coated glass showed a slow response at 0.65 μm, no such response was observed in the devices formed on Ag/Cr coated glass. Moreover the infrared quenching of photocapacitance was not observed in the silver based device at 85K. This confirms the reduced copper diffusion in the film.

9.8 CONCLUSION

The work described here has shown that the preparative conditions strongly influence the electrical and structural properties of a film which in turn affect the heterojunction characteristics. With an evaporation rate of 1.2 μm/min and T_S = 200°C, it was possible to obtain a film with columnar growth which had a resistivity of 20 ohm cm and a mobility of 11.5 $cm^2 V^{-1} s^{-1}$. An increase in evaporation rate was found to reduce the resistivity, while an increase in substrate temperature had an adverse effect. Different traps were identified from the photocapacitance studies of films grown under varying conditions. In films deposited at T_{150} a trap was found at 0.48 eV below the conduction band in addition to a few cadmium vacancies (threshold ~ 1.0 eV). The films grown at T_{200} contained cadmium vacancies and the other features of the photocapacitance spectrum were similar to those with single crystal devices. On the other hand the film deposited at T_{240} showed no sign of cadmium vacancies. Instead, a deep trap at 0.84 eV and a shallow trap at ~ 0.12 eV below the conduction band appeared. An acceptor-like state at 0.43 eV above the valence band was also found in these films.

A final important feature was the observation of a deep trap 0.946 eV below the conduction band in films deposited on Ag/Cr coated glass substrates. Similar traps were found in the Stuttgart films. At the same time the response associated with copper levels in CdS in the junctions formed on Ag/Cr substrates was much less pronounced than in those formed on film on SnO_x coated glass.

REFERENCES TO CHAPTER 9

1. G.H. Hewig, W.Hoffmann, H.Huschka, B.Schurich, J.Wörner, Proc.5th E.C.Photovoltaic Solar Energy Conf. Athens, Greece, (D.Reidel, Pub.Co.Dordrecht. 1983) p.460.
2. B.G. Caswell, Ph.D. thesis, University of Durham, 1976.
3. P.B. Hirsch et al, Electron Microscopy of Thin Crystals (Butterworth) 1965.
4. K.V. Shalimova, A.F.Andrushko, V.A.Dmitriev, and L.P.Pavlov, Sov.Phys.Crystallog. 8 (1964) p.618.
5. J.I.B. Wilson and J.Woods, J.Phys. Chem.Solids 34 (1973) p.171.
6. M.Kitada and S. Kamoshita, J.Vac.Soc.Japan 15 (1972) p.205.
7. K.H.Nicholas and J.Woods, Brit.J.Appl.Phys. 15(1964) p.783.
8. S.K. Balabanov, Compt.Rendu de l'Academie Bulgaredes Scie. 29 (1976) p.795.
9. R.H.Bube, J.Phys.Chem.Solids, 1 (1957) p.234.
10. M.A.Carter and J.Woods, J.Phys.D.Appl.Phys. 6 (1973) p.337.
11. W.Haines and R.H.Bube, Proc. 14th IEEE Photovoltaic Spec.Conf. Jan 1980, p.718.
12. S. Martinuzzi, Solar Cells 5 (1982) p.243.
13. L. Hmurick, L. Ketelsen and R.A.Serway, J.Appl.Phys. 53 (1982) p.3839.
14. H. Woodbury, J.Appl.Phys. 36 (1965) p.2287.
15. R.Hill and I.A.S.Edwards, Vacuum 27 (1977) p.277.
16. J.Vedel, M. Soubeyrand, P.Cowache and G.Leduc.Proc.P.S.E.C.Luxembourg (1977) p.601.
17. J.Dresner, and F.V.Shallcross, Solid State Electr. 1 (1962) p.205.
18. J.Dresner, and F.V.Shallcross, J.Appl.Phys. 34 (1963) p.2390.
19. F.V.Shallcross, R.C.A.Rev. (1969) p.568.
20. Y. Sakai and H.Okimura, Jap.J.Applied Phys. 3 (1964), p.144.

21. A.G.Stanley, Appl.Sol.St.Sci. 5 (1976) p.251.

22. R. Hill,'Thin Film Solar Cells' in 'Active and Passive Thin Film Devices', ed. T.J.Coutts, (Academic Press, 1978).

23. J.I.B.Wilson, Ph.D. thesis, University of Durham, 1971.

24. G.A. Somorjai and D.W. Jepson, J.Chem.Phys. 41 (1964) p.1387.

25. G.A. Somorjai and N.R. Stemple, J.Appl.Phys. 35 (1964), p.3398.

26. A.N. Nesmayov, 'Vapour Pressure of the Chemical Elements', (Elsevier,1963).

27. J. Drowart - in Proc.Int.Symp.on 'Evap. and Condens. of Solids', Ohio (1962) (Gordon and Breach).

28. G.A.Novik and S.M.Polyakov.Sov.Phys.Crystallogr. 23 (1978), p.501.

29. J. Volger, Phys.Rev.79 (1950), p.1023.

30. R.L.Petritz, Phys.Rev. 104 (1956) p.1508.

31. J.W. Orton, B.J.Goldsmith, M.J.Powell and J.A.Chapman, Appl.Phys. Lett. 37 (1980), p.557.

32. R.V.Kantariya, S. Yu Pavelets, T.M. Razykov, G.Ya Umarov and G. A. Fedorus, Sov.Phys.Semicond. 12 (1978) p.960.

33. W. Palz, J.Besson, T. Nguyen Duy, J. Vedel, Conf.Record 9th IEEE Photovoltaic Specialist Conf. Silver Spring, Maryland, U.S.A (1972) p.91.

34. A.Rothwarf and H. Windawi : Proc.14th IEEE Photovoltaic Specialists Conf. San Diego, California, Jan. 1980, p.722.

35. L.R. Shiozawa et al, Aerospace, Res.Lab.Rep.ARL 69-0155 (1969).

36. W.H.Bloss, F.Pfisterer and H.W.Schock, Proc.3rd P.S.E.C, Cannes, France (1980), p.341.

37. K.H. Norian and J.W.Edington, Thin Solid Films 25 (1981), p.53.

38. F.A.Shirland, J.Appl.Phys. 50 (1979) p.4714.

39. A. Rothwarf, Solar Cells 2 (1980), p.115.

40. W.G.Hainesand R.H.Bube, IEEE. Trans Electron Devices.Vol.ED-27, (1980) p.2133.

41. S. Martinuzzi and O. Mallem, Phys.Stat.Sol a 16 (1973) p.339.

42. L.L.Kazmerski, Solid State Electronics 21 (1978) p.1545.

43. L.M.Frass, J.Appl.Phys. 49 No.2 (1978) p.871.

44. W.R.Cook, L.Shiozawa and F.Augustine, J.Appl.Phys.4 (1970), p.3058.

45. N. Nakayama, Jap.J.Appl.Phys. 8 (1969) p.450.

46. K.W.Boer, Phys.Stat. Solidi (a) 66 (1961) p.11.

47. W.H.Bloss and F.Pfisterer, Proc.5th E.C.PSEC, Athens, Greece. 1983, p.728.

CHAPTER 10

SUMMARY AND CONCLUSIONS

The primary objective of this work was to study various forms of cadmium sulphide to identify the important fabricational, functional and operational parameters which affect the optoelectronic performance of CdS/Cu_2S solar cells. The investigations were carried out on the following forms of CdS substrate:

1. Single crystal
2. Mixed crystals of $Cd_{1-y}Zn_yS$
3. Electrophoretically deposited binderless thin films (1-2 μm) and thicker films (10 μm) with PVP as binder
4. Silk screen printed films of CdS and $Cd_{1-y}Zn_yS$ (undoped and In doped).
5. Thermally evaporated films.

The heterojunctions were formed mostly by dry barrier process. A detailed study was carried out to optimise the preparative parameters to obtain a chalcocite layer of copper sulphide, which is the desired phase of Cu_xS in CdS/Cu_xS solar cells. Oriented single crystal CdS substrates were used so that RHEED technique could conveniently be utilized for identifying the phase of the Cu_xS. Parameters such as the thickness of the CuCl, its evaporation rate, the substrate temperature and reaction time were permuted. It was found that an optimum chalcocite layer could be obtained by evaporating a layer of CuCl about 0.2 μm thick at an evaporation rate 400 Å/min on to a CdS substrate kept at 35°C, and subsequently administering a 2 min heat treatment in argon at 200°C to promote the solid state reaction between the CdS and CuCl.

RHEED studies coupled with the spectral response of the same device showed that an accurate assessment of the phase of Cu_xS layer can be

obtained from the spectral response if the temperature is lowered to 85K. At this temperature the shorter wavelength response (0.65 μm) which is due to deep copper levels in CdS diminishes, and an enhanced signal for the predominant peak associated with the Cu_xS phase (0.96 μm for chalcocite and 0.78 μm for djurleite) appears. This result was very useful for the identification of the Cu_xS phase on devices formed on CdS films where it was difficult to use the RHEED technique because of the polycrystallinity of the films.

The structural and electrical properties of the different substrates affected the device characteristics. With single crystal substrates, a procedure of mechanical polishing and subsequent etching in Conc.HCl for 30 sec was found to give optimum efficiency. With electrophoretically deposited films it was observed that the as-deposited films were highly resistive with a cubic structure. Heating in argon at 530°C for 10 min promoted a transition to the hexagonal phase. When an overlayer of $CdCl_2$ was deposited on the films, the phase transformation could be realized at 450°C. A decrease in the resistivity coincided with the phase transformation and values as low as 6×10^2 Ω-cm were obtained. Most values of electron mobility were in the range from 0.1 to 1.0 $cm^2\ V^{-1}\ s^{-1}$ with corresponding donor densities lying between 10^{14} -10^{16} cm^{-3}. The low values of mobility are caused by the potential barriers at the intergranular boundaries. These barriers were between 0.14 and 0.18 eV high. Significant grain growth took place when the temperature was raised to 600°C but was observed only in the thicker films deposited with binder. At the same time, films with binder had high resistivities of the order of 10 k Ω-cm. Films prepared from indium doped powder and subsequently treated with a $CdCl_2$ layer led to resistivities as low as 500 Ω-cm. The intergranular barrier heights were still about 0.18 eV. This was attributed to poor packing of the CdS.

The effect of $CdCl_2$ was more evident on silk screen printed films of CdS which were prepared using a thixotropic slurry obtained by mixing CdS powder swing milled for 2 min in ∿ 28% of propylene glycol (binder) and 10% $CdCl_2$. After sintering at 640°C for 60 min in argon, films were obtained with surfaces with the appearance of having partially melted. The sheet resistance of these films were as low as 1.25 kΩ/□ . In order to reduce the resistivity of the film to the extent that the need for conducting glass becomes redundant, indium doped CdS powders were used and a sheet resistance of 100 Ω/□ was obtained with 0.1 mol % indium.

$CdCl_2$ was ineffective as a flux with films prepared from $Cd_{1-y}Zn_yS$ but a mixture of $CdCl_2$ 15% + $ZnBr_2$(1%) proved to be quite good. Indium doping was beneficial in reducing the resistivity of the $Cd_{1-y}Zn_yS$ films.

The structure of the thermally evaporated films deposited on Sno_x or Ag/Cr coated glass, was mainly controlled by the substrate temperature,while the electrical properties were determined both by the evaporation rate and the substrate temperature. Better columnar growth was observed as the temperature of the substrate was increased from 150 to 200°C. However, with further increase in substrate temperature, the thickness of the film was reduced but a lateral growth of the grains was observed. RHEED patterns indicated that the films deposited at 200°C had an excellent hexagonal phase but those deposited at higher temperature were found to contain some cubic content also. The resistivity of the films deposited at the optimum temperature 200°C decreased from 900 Ω-cm to 20 Ω-cm as the evaporation rate was increased from 0.2 μm/min to 1.25 μm/min. The mobility increased with the increase in the evaporation rate and a value as high as 11.57 $cm^2\ V^{-1}\ s^{-1}$ was obtained. Interestingly the mobilities determined from the Hall measurements and from (N_D-N_A) and ρ values were found to be in good agreement indicating the nature of intergranular barriers to be the same in the lateral and longitudinal mode of electron flow.

The current voltage characteristics of an as-prepared device were of optimum shape only when the topography of the single crystal substrate exhibited well faceted hillocks. Mechanical polishing of single crystals and removal of the damaged layer in an optimal way was very important in achieving good J-V characteristics. Post barrier heat treatments were required to improve the characteristics of devices fabricated on surfaces with a spongy topography. A study of heat treatment in different ambients and for different heating times showed that the best results were obtained after heating in argon at 200^{o}C for 7 min. Air heat treated devices also improved but they were inferior to argon heated ones because of the poor fill factor. Hence a 7 min heat treatment in argon at 200^{o}C was preferred.

In thin and thick films the device parameters were affected by the growth conditions. The electrophoretically deposited films gave poorer SCC which is attributed to the intergranular barriers. In silk screen printed films although the resistivity was reduced by incorporating indium, the device characteristics were much inferior to those of cells formed on undoped material. The presence of $CdCl_2$ in undoped films reduced both the SCC and OCV. In thermally evaporated films the most distinguishable feature was the improvement in the fill factor with better columnar growth. This feature is attributed to the effect of the interfacial field which is modified by intergranular barriers in the two cases.

In junctions formed on single crystals of $Cd_{1-y}Zn_yS$ the OCV increased with the zinc content but the SCC was simultaneously reduced. Practically no difference in the FF was observed.

A comparison was also made between wet plated and dry barrier processed cells. It was found that the SCCs of the two differently prepared cells were comparable but the OCV was much higher in the dry barrier cell although its F.F. was lower. The series resistance of the wet plated cells were smaller than those of dry barrier cells, which correlates with the differences in the fill factors.

The spectral response of the heterojunctions formed on these various substrates revealed the necessity of starting with hexagonal CdS. In films which had some cubic content, an increased response near 0.7 μm appeared which was attributed to a mixture of djurleite and digenite. In addition impurities present in the CdS affected the phase of Cu_xS. In junctions formed on silk screen printed films with excess $CdCl_2$, the phase of the resultant Cu_xS was always djurleite. On the other hand in the presence of indium the main response appeared at 0.96 μm even after heat treatment. In mixed crystals the devices formed by the dry barrier process gave a predominantly chalcocite response, in contrast with those made using the wet plating technique which usually produced a mixture of chalcocite and djurleite. After heat treatment, a slow response (measured at R.T) appeared at shorter wavelength which indicated that copper had diffused into the CdS and that the stoichiometry of the Cu_xS had deteriorated. This feature was less prominent in the thermally evaporated films prepared on Ag/Cr substrates.

The photocapacitance measurements can be summarised as follows. In $CdCl_2$ treated electrophoretically deposited films the following traps were identified (1) the defect complex of a cadmium vacancy and neighbouring chlorine impurity, as with the activator of the well known self-activated luminescence centre at 1.0 eV above the valence band (2) a second deeper donor level of substitutional chlorine at 0.28 eV below the conduction band and (3) a shallow acceptor due to alkali impurity 0.18 eV above the valence band. Similar features were observed in single crystals doped with Cl or treated with $CdCl_2$.

In general, defects due to cadmium vacancies were detected ~ 0.03 eV above the valence band except in thermally evaporated films which were deposited at high substrate temperatures. Then traps at 0.17 eV and 0.84 eV below the conduction band and 0.43 eV above the valence band were more apparent. On the other hand films grown at lower temperatures revealed a

trap 0.48 eV below the conduction band. In films deposited on Ag/Cr substrates a dominant trap was observed at 0.946 eV below the conduction band and this seemed to inhibit the diffusion of copper in CdS since the heterojunction formed on these films showed no appreciable infrared quenching of photocapacitance.

The infrared quenching of photocapacitance in CdS single crystal devices revealed that copper diffuses in CdS and forms deep acceptor levels with hole ground and excited states 1.1 eV and 0.35 eV above the valence band. In those devices which were heated in air, an additional feature appeared and evidence was obtained which suggests the formation of acceptor like-states at the interface 0.2 eV below the conduction band. At the same time the measured profile of copper centres in the CdS was anomalous. Devices heated in argon exhibited pronounced maxima. This indicates that more than one diffusing species was active during the heat treatment. Thus the effects occurring at the interface are strongly influenced by the ambient during heat treatment which in turn affects the device characteristic.

In general the copper centres were revealed in the photocapacitance spectra in most of the devices formed on various forms of CdS, except for devices formed on thermally evaporated films deposited on Ag/Cr substrates. In addition a recombination centre was detected at 1.27 eV above the valence band in $Cd_{0.8}\ Zn_{0.2}S/Cu_2S$ device and also in devices formed on indium doped CdS silk screen printed films. Coincidently in both cases the SCC was much lower although the major peak in the spectral response was from chalcocite layer. It was suggested that this recombination centre was the cause of the reduced current.